CONTROL BOARD
THEORY OF OPERATION

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THEORY OF OPERATION

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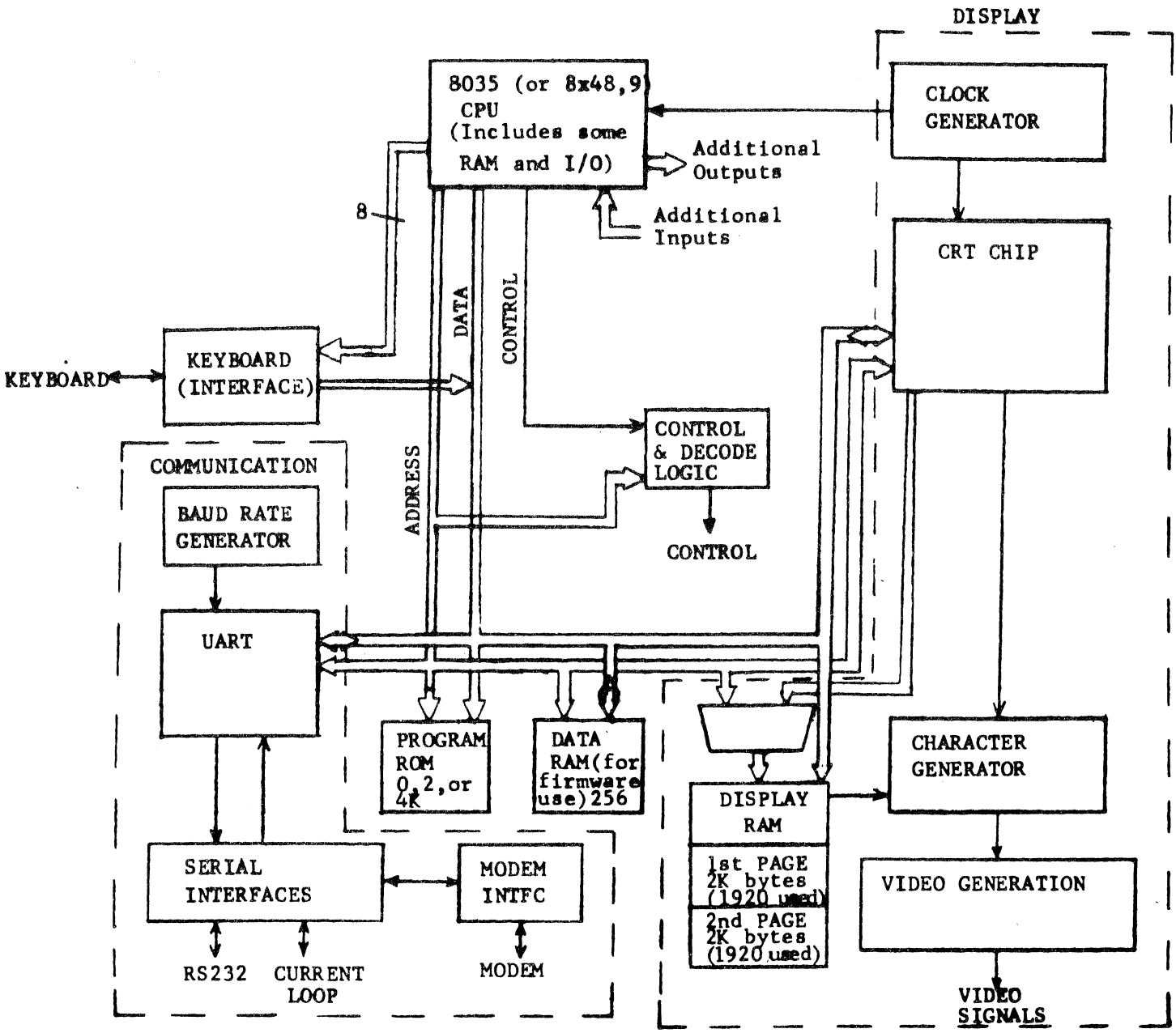
1. ARCHITECTURE OVERVIEW

The terminal's circuitry is composed of the major functional blocks as shown in Figure 1.1.

FIGURE 1.1: SYSTEM BLOCK DIAGRAM



The CPU has control over all functional sections of the terminal via a data/address bus and additional control lines. The Display and Communication sections have some circuitry that runs independently of the CPU. The Display section refreshes the video continuously, automatically. The Communication section can send and receive words at the serial level without CPU intervention.

The CPU is the Intel 8035. (See Appendix A, 8035 Specification) The bussed expansion capability of the CPU is used in order to provide external program memory, data read/write memory, display memory, and memory-mapped I/O.

Depending on firmware requirements 2K or 4K bytes of external program ROM can be accommodated. (Instead of the 8035, it is possible to use an 8048 or 8049 CPU, thus 1K bytes or 2K bytes, respectively, of external program ROM memory can be omitted.)

In addition to the internal data memory of the CPU, there is a 256 x 8 Data RAM (two 2111's) external to the CPU that is usable as read/write storage by the firmware.

The characters being displayed on the screen are accessed by the CPU via two 2K-byte blocks of read/write memory (RAM). This memory is on the same external data/address bus as the 256 x 8 Data RAM and is accessed in a similar manner. In addition to the normal read/write control lines, the Display RAM requires that the address multiplexing logic be properly controlled by the CPU for transfers to/from the display RAM.

The I/O signal lines on the CPU chip that are not used for the expansion

data/address bus, are used for various control and status functions. Additional I/O data, control, and status ports are gained by use of the expansion bus. Part of the data expansion addresses are used to implement these Input and Output capabilities. (This is known as memory-mapped I/O.) Thus, these I/O ports are treated by firmware in a manner similar to the RAM accesses, but are used for I/O transfers.

Via the I/O (direct and memory-mapped) the CPU interfaces to:

(1) the CRT chip and other display circuitry

(2) the UART and other communication circuitry

and (3) the keyboard.

The display I/O gives the CPU control over the CRT chip (including initializing the CRT chip, reading/writing the cursor position, and scrolling) and some video display circuitry (including a FORCE BLANK control).

Once initialized the CRT chip and other display circuitry can automatically perform the continuous refreshing required of the CRT by generating the video, horizontal sync, and vertical sync signals required by the CRT.

The communication I/O gives the CPU control over the UART chip (including initializing the UART's mode and sending/receiving characters on the word level) and some other communication circuitry (including printer port control, BREAK control, and control over the RS232 'ready' and 'clear' types of signals.

Once initialized the UART chip and other communication circuitry automatically perform the parallel-to-serial, serial-to-parallel, and signal level conversions required for the serial interfaces.

The Keyboard I/O allows the CPU and its firmware to scan the switch matrix that is connected to the keyboard connector.

A clock generator provides the CRT chip with the exact clock frequency required. Additionally, frequencies are tapped off for use by the CPU and the communication baud rate generator.

Accessable switches and jumpers allow the user to select many options and configurations.

Operation of the above system capabilities is described in more detail in the following sections. Page references are to the schematics of this terminal controller module.

2. OPERATION OF THE CPU INTERFACES

The CPU is the center of control in this terminal (system). This section describes the CPU, the expansion bus, and the interfaces used to control the other parts of the system. Sections 2.1 through 2.4 provides most of the information required by the firmware programmer in order to control the system.

2.1 CPU

The CPU (Central Processing Unit) is the 8035 (A54, schematic page 1). It is the Intel "Single Chip Computer", containing control circuitry for program execution, as well as program registers, read/write memory, and I/O ports. The 8035, a member of the 8048 family of single chip computers, is the version which does not contain the program ROM memory internally. The system could, if desired, use an 8048 or 8748 (each of which has 1K bytes of internal program memory) or an 8049 (which has 2K bytes of internal program memory). Using these devices can eliminate the need for all or part of the external program memory (A49 and A50, page 2). The exact configuration is an implementation and cost trade-off decision. When using internal program memory the EA (External Access) pin must be grounded by installing jumper W1 (page 1).

Appendix A contains the current 8035/8048/8748/8049 specification.

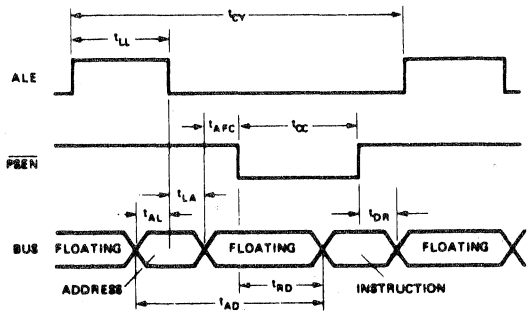
CLOCK: The CPU clock is the +6MHz (5.9535 MHz, more precisely) signal as produced by the clock generator (page 4). (See Section 5.1.) It is connected to the CPU X1 pin (A54-2, page 1). X2 requires no connection.

RESET: CPU power-up reset is effected in the normal manner by connecting the 1μF capacitor (C1) to CPU pin 4 (RESET, A54-4, page 1) and to ground. A resistor, internal to the CPU, provides the RC time constant.

ALE: The Address Latch Enable (ALE, A54-11, page 1) signal occurs once during each CPU cycle (every 2.5 μsec.). This occurs during every internal CPU cycle as well as every external CPU cycle. There are two types of external cycles: instruction fetch and data read/write. ALE is used for both in order to latch the 8 lower address bits.

$\overline{\text{PSEN}}$: Following ALE, for each external instruction fetch, the Program Store Enable ($\overline{\text{PSEN}}$, A54-9, page 1) signal occurs, see Figure 2.1. This causes a byte to be read from the program ROM (see Section 2.3.1 and 4.1).

FIGURE 2.1: INSTRUCTION FETCH FROM EXTERNAL PROGRAM MEMORY

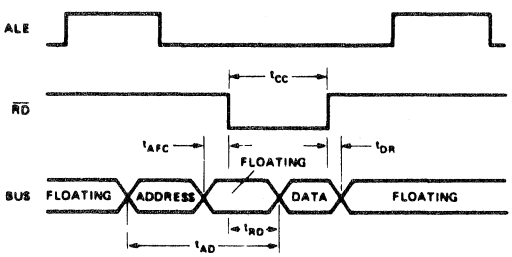


(See Appendix A for AC/DC characteristics.)

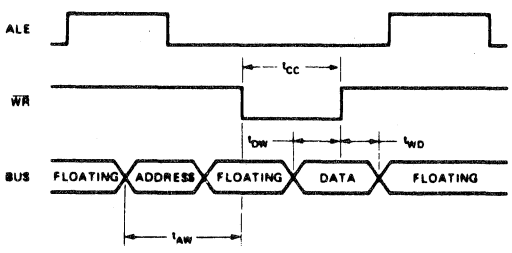
$\overline{\text{RD}}$ and $\overline{\text{WR}}$: Following ALE, for each external data read/write, either the BUS read ($\overline{\text{RD}}$, A54-8, page 1) or the BUS write ($\overline{\text{WR}}$, A54-10, page 1) signal occurs. This causes a byte to be either read from external data memory or written to external data memory, see Figure 2.2.

FIGURE 2.2:

READ FROM EXTERNAL DATA MEMORY



WRITE TO EXTERNAL DATA MEMORY



(See Appendix A for AC/DC Characteristics.)

This system uses these read/write cycles to perform external accesses to Data RAM (Section 2.3.2), Display RAM (Section 2.3.3), and memory mapped I/O (Section 2.4).

All other CPU signals are used as bus or I/O signals. They are described in other sections of this document:

PIN NAME	A54 PIN NUMBER	SIGNAL	Section
DBØ→DB7	12→19	Data Bus	2.2
P2Ø→P23	21→24	Address Signals (4MSBS)	2.2.2
P24	35	+4Hz FLASHER	2.4.1
P25	36	-DCR	2.4.2
P26	37	-PTR RDY	2.4.2
P27	38	-HALF DUPLEX	2.4.2
INT	6	-VSYNC	2.4.1
T1	39	-ADV BLANK	2.4.1
TØ	1	-CTS	2.4.2
P1Ø→P17	27→34	KEYBOARD CONNECTOR P1- 8→15	2.4.3
$\overline{\text{PROG}}$	25	-RESETUART	2.4.2

Figure 2.2.1 CPU Signals

2.2 BUS

During the external CPU cycles described in Section 2.1, the Data/Address bus signal lines carry the address information to the external components and the data information to or from those components.

2.2.1 DATA

The eight data lines +DBØ through +DB7 carry the data between the CPU pins (A54-12→19, page 1) and all of the external memory and I/O devices (pages 1 through 4). Additionally, during ALE, data lines provide the eight

least significant address signals to the D inputs of the address latch (74LS373, A51, page 1). (See timing in Figures 2.1 and 2.2). The data lines are pulled up to provide adequate high drive characteristics.

2.2.2 ADDRESS

There are twelve address lines, +AØ through +A11, used to address the memories and memory mapped I/O. The eight least significant address bits are latched (in 74LS373, A51, page 1) during ALE. The outputs of this latch provide +AØ through A7, all of which are used by the memories on pages 2 and 3. The four most significant address bits are provided by the CPU via the output pins P2Ø→P23 (A54 - 21→24) for +A8, +A9, +A10, and +A11. Four 74LS04 inverters (of A67) buffer +A11 and +AlØ, which are used for memory and memory-mapped I/O selection.

All twelve Address lines go to the program ROMs (A49 and A50) on page 2. (See Section 2.3.1.)

The data's address space is used by the RAMs and the memory mapped I/O. When +A11 is high +AØ through +A10 address the display RAM, page 3, see Section 2.3.3. When +A11 is low, and +AlØ is low, then +AØ through +A7 address the data RAM (page 2, A52 and A53, see Section 2.3.2). When +A11 is low, and +AlØ is high, then the memory mapped I/O decoder (74LS42, A58, page 1) is enabled, see Section 2.4.

2.3 MEMORY INTERFACES

2.3.1 PROGRAM ROM INTERFACE

When external program instruction memory is required, then IC locations A49 and A50 (page 2) are used. The types and configurations of ROMs used determine the operation:

	CONFIGURATION	ROM In A49	ROM In A50	JUMPERS W26	W27	W28	W29
#1:	NO EXTERNAL ROM	NONE	NONE	D.C.	D.C.	D.C.	D.C.
#2:	2K EXTERNAL ROM LOCATED 0→2K	NONE	2316E	OUT	IN	OUT	IN
#3:	2K EXTERNAL ROM LOCATED 2K→4K	2316E	NONE	OUT	IN	OUT	IN
#4:	4K EXTERNAL ROM	2316E	2316E	OUT	IN	OUT	IN
#5:	4K EXTERNAL ROM	2332	NONE	IN	OUT	IN	OUT

Figure 2.3.1 ROM Configuration D.C. = DON'T CARE

The configuration determines which instruction fetches will result in external ROM accesses. Note that an 8048, which has 1K of internal program memory, will only execute external fetches for the 1K to 4K address range (unless the EA pin is pulled high). Section 4.1 describes the operation of the ROMs.

2.3.2 DATA RAM INTERFACE

The 256 x 8 Data RAM is selected when the external address is:

A11	A10	A9	A8	A7 A0	
0	0	D.C.	D.C.	byte select	D.C. = DON'T CARE

which, in hex, is 0XX = 1XX = 2XX = 3XX, where XX is the byte select.

2.3.3 DISPLAY RAM INTERFACES

There are two 2048 byte display RAM PAGES. (Only 1920 bytes are actually displayed in standard operation.) (four 2114's; A6, A8, A10, and A12; on schematics page 3) can be addressed when +PG SEL is set true (output bit 0

to memory mapped I/O location 4ØC; see Section 2.4.1.). PAGE 2 (four 2114's; A5, A7, A9, and A11; on schematics page 3) can be addressed when +PGSEL is set false (i.e., to zero).

For whichever of the two PAGEs is enabled (by +PGSEL), the Display RAM is selected when the external address is:

A11	A10→AØ
1	byte select

which, in hex, is 8XX—FXX.

Performing a read or write to external data memory in this address range will automatically override the refresh circuitry's addressing of the Display RAM, giving the CPU priority at all times. Section 2.4.1 describes how the CPU can be synchronized with the refreshing to accomplish accesses only during blanking periods.

Due to hardware implementation efficiencies the addressing of the 1920 characters being displayed on the CRT is not a direct linear mapping within the 2048 byte Display RAMs. Table 2.1 shows 80 character by 24 line display with the corresponding Display RAM locations for each character.

2.4 I/O CONTROL AND STATUS INTERFACES

All memory mapped I/O ports use the 74LS42 decoder (A58, page 1) to detect the +A2, +A3, +A10, and +A11 address lines. +A2 and +A3 select which port is being addressed, while the combination of +A11 = 0 and +A10 = 1 is required for all memory mapped operations. Additionally the keyboard circuitry uses +AØ and +A1, and the CRT chip uses +AØ, +A1, +A4, and +A5 for additional addressing.

TABLE 2.1

Corresponding Display RAM Addresses
for the 80 Character x 24 Line Display

CHAR ROW DEC	CHAR ROW HEX	CHAR POSITION: DEC	0----------15	16----------31	32----------47	48----------63	64----------79	ROW DEC.
		CHAR POSITION: HEX	0----------F	10----------1F	20----------2F	30----------3F	40----------4F	
0	0		800----------83F				E00----------E0F	0
1	1		840----------87F				E40----------E4F	1
2	2		880----------8BF				E80----------E8F	2
3	3		8C0----------8FF				EC0----------ECF	3
4	4		900----------93F				F00----------F0F	4
5	5		940----------97F				F40----------F4F	5
6	6		980----------9BF				F80----------F8F	6
7	7		9C0----------9FF				FC0----------FCF	7
8	8		A00----------A3F				E10----------E1F	8
9	9		A40----------A7F				E50----------E5F	9
10	A		A80----------ABF				E90----------E9F	10
11	B		AC0----------AFF				ED0----------EDF	11
12	C		B00----------B3F				F10----------F1F	12
13	D		B40----------B7F				F50----------F5F	13
14	E		B80----------BBF				F90----------F9F	14
15	F		BC0----------BFF				FD0----------FDF	15
16	10		C00----------C3F				E20----------E2F	16
17	11		C40----------C7F				E60----------E6F	17
18	12		C80----------CBF				EA0----------EAF	18
19	13		CC0----------CFF				EE0----------EEF	19
20	14		D00----------D3F				F20----------F2F	20
21	15		D40----------D7F				F60----------F6F	21
22	16		D80----------DBF				FA0----------FAF	22
23	17		DC0----------DFF				FE0----------FE0	23

The 74LS42 (A58) decoder must also be enabled by the delayed signal which is the OR of the RD and WR signals. (This delay provides adequate data setup time for the UART.)

The $\overline{WR}$ signal provides the "C" input (A58-1) to the decoder, which causes decoder outputs Ø→3 to be "I/O writes" and 4→7 to be "I/O reads."

I/O beyond the memory mapped I/O comes directly from CPU I/O pins. All of the I/O is described in Sections 2.4.1 through 2.4.4, below.

2.4.1 CRT CHIP AND DISPLAY CONTROL

CRT CHIP: The CRT chip responds to the following memory-mapped I/O addresses:

Figure 2.4.1a CRT Chip Addressing

ADDRESS BIT												ADDR IN	RD	CRT CHIP
11	10	9	8	7	6	5	4	3	2	1	Ø	HEX*	or WRT	OPERATION
0	1	D.C.	D.C.	D.C.	D.C.	X	X	0	0	X	X			SELECT CRT CHIP
0	1	D.C.	D.C.	D.C.	D.C.	0	0	0	0	0	0	400	WRT	CONTROL REG Ø
↑	↑	↑	↑	↑	↑	0	0	↑	↑	0	1	401	WRT	" " 1
						0	0			1	0	402	WRT	" " 2
						0	0			1	1	403	WRT	" " 3
						0	1			0	0	410	WRT	" " 4
						0	1			0	1	411	WRT	" " 5
						0	1			1	0	412	WRT	" " 6
						0	1			1	1	413	RD	Processor Self Load NOT USED
						1	0			0	0	420	RD	Read Cursor Char Addr.
						1	0			0	1	421	RD	Read Cursor Line Addr.
						1	0			1	0	422	RD	Reset
						1	0			1	1	423	RD	Up Scroll
						1	1			0	0	430	WRT	Load Cursor Char Addr.
						1	1			0	1	431	WRT	Load Cursor Line Addr.
↓	↓	↓	↓	↓	↓	1	1	↓	↓	1	0	432	RD	Start Timing Chain
0	1	D.C.	D.C.	D.C.	D.C.	1	1	0	0	1	1	433	RD	Non-Processor Self Load NOT USED

D.C. = DON'T CARE *Assumes DON'T CARES = Ø

The above CRT Chip operations are as defined in the 5027 CRT CHIP specifications, Appendix B. In order to attain the 24 lines of 80 characters each at either 50 Hz or 60 Hz, the Control Registers should be loaded by the

CPU as follows:

Figure 2.4.1b Control Register

CONTROL REGISTER	VALUE (IN HEX)	
	50 Hz	60 Hz
Ø	68	68
1	43	43
2	4D	4D
3	97	97
4	22	Ø7
5	32	17
6	17	17

Section 5.2 describes the operations directed by the above control registers.

-VSYNC: The CPU receives the vertical synchronizing signal at the INT input of the CPU (A54-6, page 1). This allows the CPU firmware to perform timed operations based on the very precise 50 Hz or 60 Hz -VSYNC signal.

-ADVBLANK: The CPU can synchronize to the display's blanking time by sensing this signal. This allows the CPU to perform Display RAM accesses only during blank times, if desired, to avoid visable effects on the display. When the CRT CHIP is programmed with the standard values (as listed above) the -ADVBLANK signal is 25 character times long (active low) during horizontal blanking. However, Display RAM access by the refresh circuitry starts one character time before the end of -ADVBLANK. This means that from the detected leading edge of -ADVBLANK the CPU has 24 character times (less the sampling period) during which it can be guaranteed blanking. Each character time is 588 nsec. which mean the CPU has 14.1 μsec (less the T1 sampling period) to perform the Display Ram read or write without effecting the refresh logic.

+4Hz FLASHER: The CPU firmware is to generate this output at P24 (A54-35) by using the -VSYNC interrupt input (see above) and dividing down appropriately. +4Hz FLASHER is used to flash the Cursor (if jumpered to do so by inserting W25) and is divided by 2 to generate the 2 Hz signal used to gate the blinking video field(s) on and off.

+FORCE BLANK: The CPU firmware can force the video to be blanked by outputting a 1 on this bit. +FORCE BLANK is part of the 74LS174 Output Port (A47-15, page 1) which is loaded by performing the memory-mapped I/O write to location 40C (HEX) or, more precisely,

Address Bit:	11	10	9	8	7	6	5	4	3	2	1	0
Value:	0	1	DC	DC	DC	DC	DC	DC	1	1	0	0

DC = DON'T CARE

Data bit 5 is the +FORCE BLANK bit. Firmware would normally keep an image of this port in RAM, such that only the bits of interest can be changed without affecting the others. A summary of output port 40CH is:

Output to 40CH

Bit	Signal	
7	DON'T CARE	
6	DON'T CARE	
5	+FORCE BLANK	(see above)
4	+SEL LPT	(see Section 2.4.2)
3	-BREAK	(" " ")
2	-RQS	(" " ")
1	+BEEP	(" " 2.4.4)
0	+PG SEL	(see below)

Figure 2.4.1c Output Port 40CH Summary

+PG SEL: The CPU firmware selects which 2048-byte PAGE of display RAM is to be displayed. (Only 1920 characters are actually displayed.) This also selects which RAM is accessed by the CPU via the Display RAM addresses (Section 2.3.3). +PG SEL is set to a 0 to select PAGE 1 and is set to a 1 to select PAGE 2. This control bit is data bit 0 on output port 40CH as described under +FORCE BLANK, above.

2.4.2 UART AND COMMUNICATION CONTROL

UART CHIP: The UART Chip responds to the following memory-mapped I/O addresses:

ADDRESS BIT												ADDR IN HEX*	READ or WRT	UART OPERATION
11	10	9	8	7	6	5	4	3	2	1	0			
0	1	DC	DC	DC	DC	DC	DC	0	1	DC	DC	404	READ	Read Data Enable
0	1	DC	DC	DC	DC	DC	DC	1	0	DC	DC	408	WRT	Write Data Strobe
0	1	DC	DC	DC	DC	DC	DC	1	0	DC	DC	408	READ	Status Word Enable

Data Bit	Status
3	FE, FRAME ERROR
2	PE, PARITY ERROR
1	TBMT, TRANSMIT BUFFER EMPTY
0	DTA, DATA AVAILABLE

DC = DON'T CARE
* Assumes DON'T CARES = Ø

Figure 2.4.2 UART Chip Address

The above UART Chip operations are as defined in the UART specification in Appendix C. The hardware operation of the UART interface is described in Section 6.

+RESET UART: The CPU firmware can pulse this line by using I/O expander instructions (which strobe the $\overline{\text{PROG}}$ output pin of the CPU, A54-25, page 1). This signal is connected to the UART's RESET input.

+SEL LPT: The CPU controls this signal by performing a memory-mapped output operation to address 40CH with bit 4 being +SEL LPT:

Output 40CH

Bit	Signal	
7	DON'T CARE	
6	" "	
5	+FORCE BLANK	(Section 2.4.1)
4	+SEL LPT	
3	-BREAK	(see below)
2	-RQS	(see below)
1	+BEEP	(see Section 2.4.4)
0	+PG SEL	(" " 2.4.1)

When set to 1, the +SEL LPT control line enables the line printer serial communication transmitter (connector P4-3, PRT DATA (RS 232), page 2) and disables the normal transmitter data driver (connector P3-2, TXD (RS 232), page 2). When set to Ø, +SEL LPT disables the printer transmitter and enables the normal serial transmitter. Additionally, +SEL LPT selects the line printer serial baud rate (as determined by switches S3) when set to a 1, or the normal serial baud rate (as determined by switches S1). This allows the printer and normal serial interfaces to have independent baud rates. (Note that the UART does not receive serial data at the normal baud rate when the printer is enabled.)

-BREAK: This signal is controlled by the CPU using address 4ØCH, bit 3 (see above). -BREAK, when set to Ø forces the selected serial transmit line to the "break" state. This allows the CPU firmware to create the desired Break condition for the desired duration.

-RQS: This output bit (address 4ØCH, bit 2, see above) directly drives the normal terminal serial interface's RTS (Request to Send, P3-4, page 2)

which also goes to the modem connector (P6-4, page 2). Additionally this can drive DTR (P3-20, page 2), if enabled using switch S5-3, 12. This bit can also drive the printer's serial port TERM RDY lines P4-8 and/or P4-6 (page 2) which can be connected by jumpers W12 and W13, respectively.

-DCR: The CPU can input -DCR on I/O pin P25 (A54-36, page 1). This signal can come from any of 3 different places: (1) "DCR (RS232)" at P3-6 (page 2) which can be enabled by switch S5-1, 14; (2) "DCR (RS232)" at P3-8 (page 2) which can be enabled by switch S5-2, 13; and (3) Modem connector P6-7 (page 2).

-PTR RDY: The firmware inputs this signal via the CPU I/O pin P26 (A54-37, page 1). It is the Printer Ready signal derived from connector P4-20 (+PTRRDY (RS232), page 2).

-HALF DUPLEX: The CPU firmware reads CPU I/O pin P27 (A54-38, page 1) to determine the Full/Half Duplex mode. When -HALF DUPLEX is Ø the firmware should enter half duplex mode and when 1 the terminal should be in full duplex mode. -HALF DUPLEX is derived from switch S2-3,18 (page 1), one side of which is grounded.

2.4.3 KEYBOARD I/O INTERFACES

The outputs to the Keyboard matrix consist of the 8 lines from the CPU I/O pins P1Ø→P17 (A54-27→34, page 1) which are connected to Keyboard connector pins P1-8 through P1-15, respectively. There are 12 inputs from the matrix and 4 inputs from individual keys. All inputs are pulled up by 1K ohm resistors to +5V.

Figure 2.4.3 Keyboard I/O Interfaces

The CPU reads Keyboard inputs via the following memory-mapped I/O reads:

ADDRESS BIT 11	10	9	8	7	6	5	4	3	2	1	0	ADDR IN HEX*	KEYBOARD INPUTS (P1 Connector Pins) On Data Bits 7	6	5	4	3	2	1	0
0	1	DC	DC	DC	DC	DC	DC	1	1	0	0	40C	+50Hz	(ALPHA) 3	26	(SHFT) 4	(CTL) 6	(FUNC) 5	16	20
								1	1	0	1	40D	"	"	25	"	"	"	17	21
								1	1	1	0	40E	"	"	24	"	"	"	18	22
0	1	DC	DC	DC	DC	DC	DC	1	1	1	1	40F	"	"	7	"	"	"	19	23

Non Keyboard

DC = DON'T CARE
* Assumes DON'T CARES = 0

Note that the 4 individual keys are input on all four addresses. "-50 Hz" is also input with these input operations and is to determine the terminal's refresh rate upon power up, as described in Section 2.4.4.

Appendix D provides the descriptions of keyboard matrix with which this system has been interfaced.

2.4.4 OTHER I/O INTERFACES

-50 Hz: As described under Section 2.4.3, above, this signal can be read by the CPU firmware on memory-mapped I/O address 40C (as well as many others) on data bit 7. The firmware should sense this bit during power-up and initialize the CRT chip accordingly (see Section 2.4.1). When -50 Hz = 0 then the 50 Hz mode should be established, else the 60 Hz mode. This signal is derived from switch S2 pins 17 and 4 (pin 4 is grounded).

+BEEP: The CPU firmware can control the beeper (audio signal, 1200 Hz) with bit 1 of the memory-mapped I/O write to address 40CH (see, also, Sections 2.4.1 and 2.4.2 for the other control bits affected). The +BEEP signal is

gated with the +1200 Hz signal (on page 1 with 74LS00, A61-1,2,3) which is then inverted to drive transistor Q2 which, in turn, drives the 8 ohm speaker connected to P7-1,2. When +BEEP is Ø the gating is such that the +1200 Hz is removed and the transistor Q2 is put in the off (non-conducting) state.

3. OPERATION OF JUMPERS AND SWITCHES

Presented below is a summary of the switches and jumpers used in the system. Included are short descriptions of their functions and references to other pertinent sections of this document. Though redundant, this section should provide quick reference for software, hardware, and systems technical personnel.

JUMPER #	DESCRIPTION		Schem. Page	Reference Sections	Comments
	INSERTED	REMOVED			
W1	USE INTERNAL PROGRAM MEMORY (ROM)	USE EXTERNAL PROGRAM MEMORY (ROM)	1	2.1	
W2					NOT USED
W3					"
W4					"
W6	P3 CONN: CURRENT LOOP SEND SHORT 510 SERIES	KEEP 510 IN SERIES	2	6.3	▷2
W7					NOT USED
W8					"
W9					"
W10					"
W11					"
W12	P4 CONN: TERM RDY (RS232C) SENT ON P4-6	P4-6 NOT CONN	2	6.3	
W13	P4 CONN: TERM RDY (RS232C) SENT ON P4-8	P4-8 NOT CONN	2	6.3	

Table 3.0 Summary of Switches and Jumpers

JUMPER #	DESCRIPTION		Schem. Page	Reference Sections	Comments
	INSERTED	REMOVED			
	P3 CURRENT LOOP SEND				
W14	CONN "COLLECTOR END" TO P3-25	"COLLECTOR END" not CONNECTED TO P3 -25	2	6.3	2
W15	CONN "EMITTER END" TO P3-25	"EMITTER END" NOT CONN TO P3-25	2	6.3	2
W16	CONN "EMITTER END" TO P3-13	"EMITTER END" NOT CONN TO P3-13	2	6.3	2
W17	CONN P3-13 TO GND	P3-13 NOT CONN TO GND	2	6.3	2
W22					Not used
W23					Not used
W24					Not used
W25	CURSOR FLASHES OFF ON (INVERSE VIDEO)	CURSOR DOES NOT FLASH AND IS INVERSE VIDEO	5	5.4	
W26	for 2332 ROM at A49	for all others	2	2.3.1, 4.1	
W27	for 2316E, 8316E, 2716 ROMs at A49 or A50	for all others	2	2.3.1, 4.1	
W28	for 2332 ROM at A49	for all others	2	2.3.1, 4.1	
W29	for 2316E, 8316E, 2716 ROMs at A49 or A50	for all others	2	2.3.1, 4.1	
W30	For all character generator PROMs	For no standard character generator PROMs	5	5.3	

JUMPER #	DESCRIPTION		Schem. Page	Reference Sections	Comments
	INSERTED	REMOVED			
	OPTIONAL RESISTORS				
R28	P3 CONN: CURRENT LOOP SEND, PULLS HIGH END TO +12V.	NOT PULLED UP	2	6.3	▷2

SWITCH #	PINS	DESCRIPTION CLOSED	OPEN	Schem. Page	Reference Sections	Comments
COMMUNICATION PORT BAUD RATE SELECT (P3-2 and 3)						
S1	1-2	19,200	NOT 19,200	6	6.1	
	2-1	9,600	NOT 9,600	6	6.1	
	3-1	4,800	NOT 4,800	6	6.1	
	4-17	2,400	NOT 2,400	6	6.1	
	5-16	1,200	NOT 1,200	6	6.1	
	6-15	600	NOT 600	6	6.1	
	7-14	300	NOT 300	6	6.1	
	8-13	150	NOT 150	6	6.1	
	9-12	75	NOT 75	6	6.1	
S1	10-11	110	NOT 110	6	6.1	
S2	10-11	SHORT OUT 270 IN SERIES WITH CHARACTER VIDEO	KEEP 270 IN SERIES (FOR COMPOS VIDEO)	5	5.4	OPEN FOR COMPOS VID (SEE S2-1,20)
	2-19	SELECT LOWER HALF OF CHARACTER GENERATOR	SELECT UPPER HALF OF CHARACTER GENERATOR	5	5.3	
	3-18	HALF DUPLEX	FULL DUPLEX	1	2.4.2	
	4-17	50Hz	60Hz	1	2.4.4	
	5-16	PARITY IN TRANS AND RCV	NO PARITY	2	6.2; C	(see also S2-9,12)
	6-15	1 STOP BIT (TRANS)	2 STOP BITS (TRANS)	2	6.2; C	
	7-14 NB1 8-13 NB2	BITS PER CHAR	S2-7,14: CLOSED OPEN CLOSED OPEN S2-8,13: CLOSED CLOSED OPEN OPEN #BITS = 5 6 7 8	2	6.2; C	
	9-12	SEND AND RECEIVE: ODD PARITY	EVEN PARITY	2	6.2; C	(see also S2-5,16)
S2	1-20	a)+VIDEO P2-4 GETS COMPOS SYNC TOO	a)+VIDEO P2-4 HAS NO SYNC's	5	5.4	S2-10,11 SHOULD BE OPEN FOR VIDEO WITH COMPOS SYNC
		b)+TTL VIDEO BECOMES VIDEO WITH COMPOS SYNC(P2-6)	b)+TTL VIDEO P2-6 IS ONLY COMPOS SYNC			

SWITCH #	PINS	DESCRIPTION CLOSED	OPEN	Schem. Page	Reference Sections	Comments
S3	1-20	19,200	NOT 19,200	6	6.1	1
	2-19	9,600	NOT 9,600	6	6.1	
	3-18	4,800	NOT 4,800	6	6.1	
	4-17	2,400	NOT 2,400	6	6.1	
	5-16	1,200	NOT 1,200	6	6.1	
	6-15	600	NOT 600	6	6.1	
	7-14	300	NOT 300	6	6.1	
	8-13	150	NOT 150	6	6.1	
	9-12	75	NOT 75	6	6.1	
S3	10-11	110	NOT 110	6	6.1	
S5	1-14	CONN P3: RECEIVE DCR(RS232C) FROM P3-10	DO NOT RECEIVE DCR FROM P3-10	2	6.3	1
	2-13	CONN P3: RECEIVE DCR(RS232C) FROM P3-8	DO NOT RECEIVE DCR FROM P3-8	2	6.3	
	3-12	CONN P3: P3-20 (DTR) DRIVEN BY SAME AS RTS (P3-4				1
	4-11	CONN P3: P3-20 (DTR) PULLED TO +12V VIA 3.3K	P3-20 (DTR) NOT PULLED HIGH			
	5-10 6-9	CONN P3: RECEIVE SERIAL DATA RS232C P3-3	DO NOT RECEIVE SERIAL DATA RS232C P3-3	2	6.3	1
S5	7-8	CONN P3: RECEIVE SERIAL DATA CURRENT LOOP P3-12, 24	DO NOT RECEIVE SERIAL DATA CURRENT LOOP P3-12,24	2	6.3	

1 CLOSED CONDITIONS OF SWITCHES WITHIN INDICATED SWITCH GROUP ARE MUTUALLY EXCLUSIVE

2 MUTUALLY EXCLUSIVE CURRENT LOOP SEND CONNECTIONS FOR P3

P3 CONN: ISOLATED (W6, W-14, W-16 INSERTED) VS. 1-SIDE GND (R28, W15, W17 INSERTED)

4. PROGRAM MEMORY OPERATION

The operation of the hardware for the program memory is described in sections 4.1 (program ROM) and 4.2 (data RAM). The functional interface for system and firmware reference is described in sections 2.3.1 and 2.3.2.

4.1 PROGRAM ROM

When external program memory is required by the CPU, the (P)ROMs at locations A49 and A50 (page 2) are used.

The two ROMs have the 11 address lines and the 8 output data lines in common. The lower 8 address lines (+A7→+AØ) come from the address latch (A51, page 1) and +A10, +A9, and +A8 come from CPU port 2: bit 2 (A54-23, buffered), bit 1 (A54-22) and bit Ø (A54-21), respectively. The output data lines are connected to the CPU data bus (+DB7→+DBØ).

If the ROMs are 2316E types (i.e., 16K bits) then memory address bit A11 (derived from CPU port 2 bit 3, A54-24) selects which ROM is enabled when -PSEN goes active. +A11 and its inverse are each gated with -PSEN (page 1, A66-1,2,3 and A66-11,12,13) yielding -ROM1CS or -ROMØCS, one of which goes active when -PSEN goes active. -ROMØCS goes active for +A11=Ø and -ROM1CS goes active for +A11=1. -ROMØCS selects the ROM at A50 (page 2, A50-20). -ROM1CS selects the ROM at A49 (A49-20). Note that for 2316E-type ROMs jumper W29 is inserted (and W28 is not) in order to pass the -ROM1CS signal. Jumper W27 must be inserted (and W26 not inserted) for 2316E ROMs. This provides pin 21 (on A49 and A50) with +5V, which is required for PROMs (2716 or 2758) that may be used, and provides the high logic level for the ROMs that have a positive chip select at this pin.

If a 2332-type (i.e., 32K bit) ROM is used then jumper W28 and W26 must be inserted while omitting W29 and W27. This provides A49-20 with -PSEN directly such that this ROM is selected on every -PSEN cycle, not just when +A11=1. Jumper W26 connects +A11 to A49-21 providing the ROM with the required 12th address bit.

The negative chip select at pin 18 (on A49 and A50) is permanently grounded.

4.2 DATA RAM

The 2111A (or 8111A) RAM chips (page 2, A52 and A53) comprise a 256 x 8 block of read/write memory, with A52 providing for data bits 7, 6, 5, and 4 and A53 for bits 3, 2, 1 and Ø. This data leaves and enters via IO1→IO4 (pins 11→14) on A52 and A53, and is connected to the CPU data bus +DB7 +DBØ (see page 2). The required 8 address bits are +A7→+AØ.

This 256 x 8 RAM is enabled when +A10 and +A11 are both logic Ø by generating -DSCS (page 1, A66-4,5,6) which connects to A52-15 and A53-15.

-DSCS in conjunction with -RD pulse (from the CPU, page 1, A54-8) causes the RAMs' outputs to be enabled (via A52 and A53 pin 9). During -RD the addressed data is then driven onto the data bus.

-DSCS in conjunction with -WR pulse (from the CPU, A54-10) causes the RAMs (via A52 and A53 pins 16) to write the 8 bits from the data bus at the addressed internal locations.

5. DISPLAY OPERATION

5.1 CLOCK GENERATION

The crystal oscillator (page 4) uses an astable 74S04 configuration to generate the 23.814 MHz signal (at A55-4). The crystal is series resonant at 23.814 MHz. The 74LS109 flipflop (A56-2→7) divides the basic clock by 2 to provide an 11.907 MHz "square" wave, +CLK (A56-6) and -CLK (A56-7). These two signals go on to the Video Generation circuitry on page 5 (see Section 5.4) to provide the gating and shifting clock for the basic dot of the video generation.

See Figure 5.1 for the timing diagram.

The 74LS163 dot counter (page 4, A57) provides the display character clock (+DC CARRY, A57-15) to the video generation logic (page 5) and its frequency equivalent, -DC2 (A55-12), to the 5027 CRT Chip (at A23-12, page 4). The counter's bits Q_A, Q_B, and Q_C generate the dot counter bits +DCØ, +DC1, and +DC2, respectively. +DCØ and +DC2 are used on page 5 by the video generation circuitry (Section 5.4). +DC1 generates an asymetrical 3.402 MHz (11.907 ÷ 3.5) signal which is used on page 6 by the baud rate generator (Section 6.1).

+CLK is divided by 2 by the 74LS109 (page 4, A56-10→15) to generate +6MHz (actually 5.9535 MHz) on A56-10. +6MHz goes to the CPU (page 1, A54-2) to provide the basic CPU clock.

5.2 CRT CHIP OPERATION

The CRT 5027 Video Timer and Controller ("VTAC" or "CRT CHIP") for SMC Microsystems Corporation is described in detail by the specification in Appendix B. This section describes the CRT Chip's specific operation

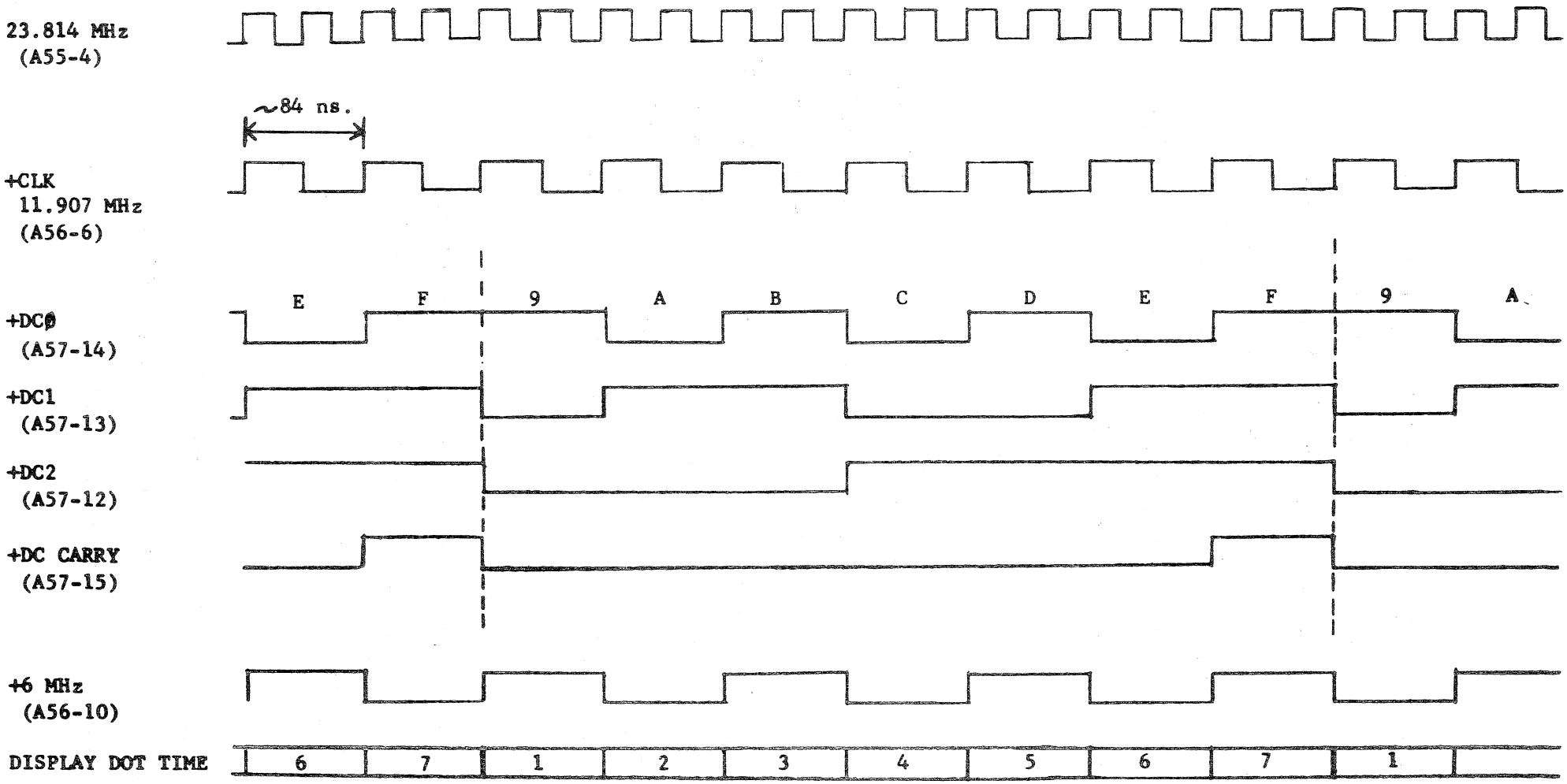


FIGURE 5.1
CLOCK GENERATION TIMING DIAGRAM

when the control registers are programmed for this system as described in Section 2.4.1.

Clock Input: The clock input (DCC, A23-12, page 4) to the CRT chip is at the display character rate. It is the same as the inverse of +DC2 in Figure 5.1. The CRT Chip Specification in Appendix B shows timing of the output signals relative to the input clock.

Hardware Addressing Operation: Accessing the CRT CHIP (page 4) is performed by presenting the proper address inputs (A3→AØ, A23-2,1,40, and 39) and then providing a negative strobe at the data select ($\overline{DS}$, A23-9). Depending on the address inputs the chip performs a read (DB7→DBØ, A23-18→25, drive the CPU data bus +DB7→+DBØ) or a write (the chips DB7 DBØ accept data from the CPU data bus +DB7→+DBØ). Of the 16 addressable I/O registers (ports in the CRT CHIP) 9 are output (write) and 7 are input (read) ports. The address table in Section 2.4.1 shows which ports are write and which are read. Note that the address lines connected to the chip's address pins are: +A5, +A4, +A1 and +AØ to the chip's A3, A2, A1, and AØ, respectively. Since the CRT Chip wants only one control strobe (i.e., not both a read and a write strobe) the read and write outputs of the I/O decoder (page 1, A58) for address decodes "400" are logically OR'd (by A43-11,12,13, page 1) yielding -SEL CRT CHIP. This signal provides the data select for the CRT Chip (A23-9, page 4). The "400" decoded signal, in conjunction with the 4 address lines, accounts for the I/O address locations (as presented in the table in Section 2.4.1).

Operation of CRT Chip programming: As stated in Section 2.4.1 the 7 control registers must be programmed for either 50 Hz or 60 Hz for standard operation:

CONTROL REGISTER	VALUE (IN HEX)	
	50 Hz	60 Hz
Ø	68	68
1	43	43
2	4Ø	4Ø
3	97	97
4	22	Ø7
5	32	17
6	17	17

Variations from this might be possible for special cases, but for 24 lines of 80 displayed characters (at 50 Hz or 60 Hz refresh rates) it is necessary to use these values with the clock generation and video generation circuitry provided in this system.

The above control register values provide the following parameters to the CRT Chip (see also the CRT Chip timing, Figure 5.2):

5.2.1 -- Control Register Ø

Bits 7→Ø = N; Horizontal Line count where Total Characters/Line = N + 1.

50 Hz Total Characters/Line = 68_{16} + 1

= 104_{10} + 1

= 105

60 Hz --Same--

5.2.2 -- Control Register 1

Bit 7; Interlaced/Non-Interlaced

where 1 = Interlaced; Ø = Non-Interlaced

50 Hz Bit 7 = Ø, Non-Interlaced

60 Hz --Same--

Bits 6→3 = N; Horizontal Sync Width

where Horiz Sync Width Character Times = N

(N = 1→15; N = Ø, disallowed)

50 Hz Horiz Sync Width Char Times = 8

60 Hz --Same--

Bits 2→Ø = N; Horizontal Sync Delay

where Horiz Sync Delay Char Times = N

(N = 1→7; N = 0, disallowed)

50 Hz Horiz Sync Delay Char Times = 3

60 Hz --Same--

5.2.3 -- Control Register 2

Bit 7, not used (= Ø)

Bits 6→3 = N; Scans/Data Row

Where Scans/Data Row = N + 1

50 Hz Scans/Data Row = 9 + 1
= 10_{10}

60 Hz --Same--

Bits 2→Ø = T; Characters/Data Row

where T is defined in a table in the CRT Chip Specification (Appendix B, last page).

For DB 2 = 1, DB1 = Ø, DB Ø = 1 the

Characters per Data Row = 80

50 Hz Characters/Data Row = f(T)
= f(5)
= 80_{10}

60 Hz --Same--

5.2.4 -- Control Register 3

Bits 7, 6 = T; Skew Bits (Refer to 5.4)

where T is defined in a table in the CRT Chip Specification (Appendix B, last page).

For DB 7 = 1, DB 6 = Ø the Skew Bits

are Sync/Blank Delay = 1 Character Time

Cursor Delay = Ø Character Time

50 Hz Skew Bits = f(T)

= $f(2_{10})$

= Sync/Blank Delay of 1 Char Times

Cursor Delay of no Char Times

60 Hz --Same--

Bits 5→Ø = N; Data Rows/Frame

where Number of Data Rows = N + 1

(N = Ø 63)

50 Hz Number of Data Rows = 17_{16} + 1

= 23_{10} + 1

= 24

60 Hz --Same--

5.2.5 -- Control Register 4

Bits 7→Ø = N; Scans/Frame

where, in non-interlaced mode,

Scans/Frame = 2N + 256

50 Hz Scans/Frame = $2 \cdot 22_{16} + 256_{10}$

= $2 \cdot 34_{10} + 256_{10}$

= $68_{10} + 256_{10}$

= 324_{10}

60 Hz Scans/Frame = 2·Ø7 + 256

= 14 + 256

= 270_{10}

5.2.6 -- Control Register 5

Bits 7→Ø = N; Vertical Data Start

where N = number of raster lines after leading edge of vertical sync of vertical start position.

50 Hz Vertical Data Start (raster lines) = 32_{16}

= 50_{10}

60 Hz Vertical Data Start (raster lines) = 17_{16}

= 23_{10}

5.2.7 -- Control Register 6

Bits 7, 6, not used (= Ø)

Bits 5→Ø = N; Last Displayed Data Row

where N = Address of last displayed data row, N = 0 to 63

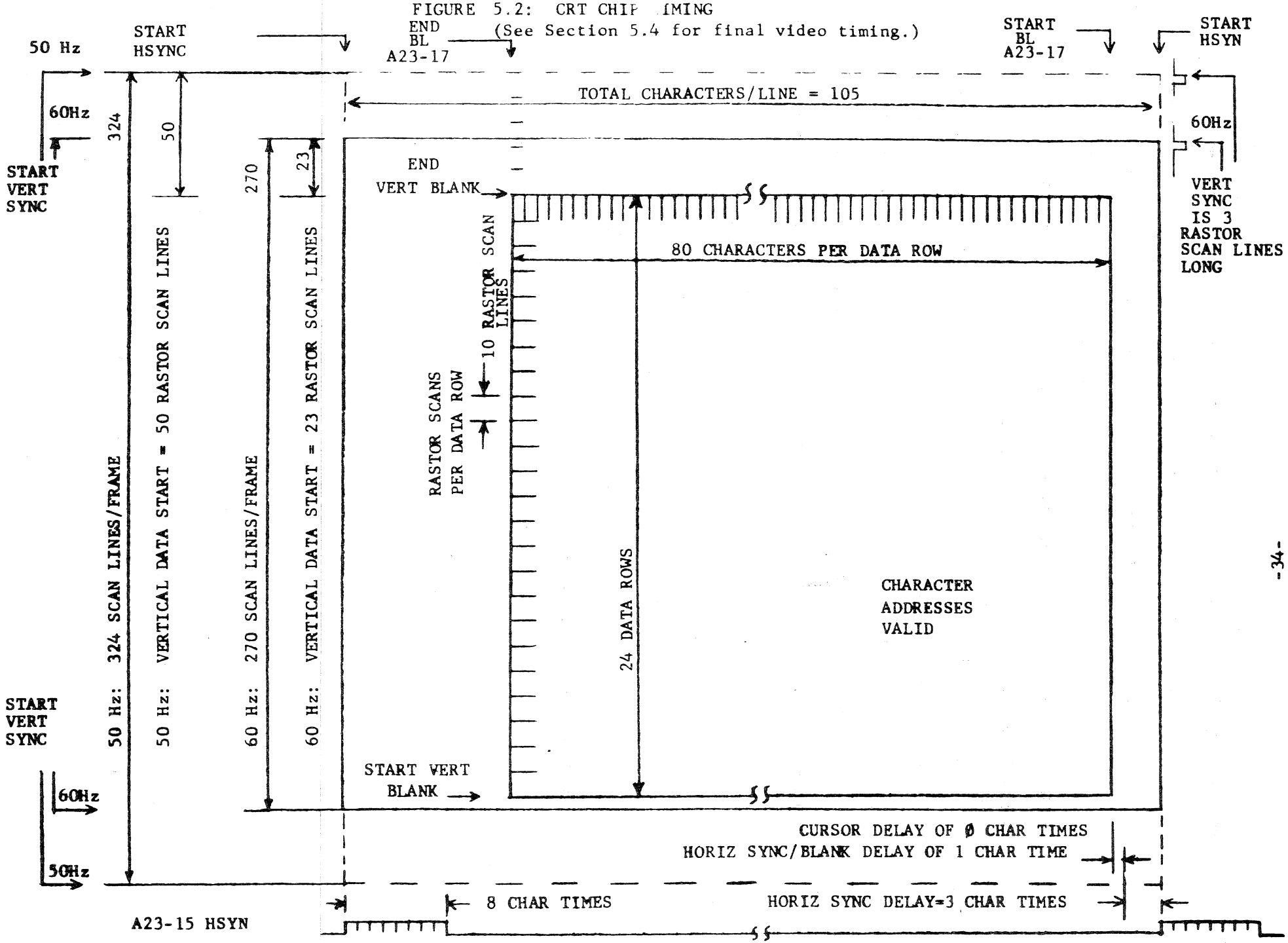
50 Hz Last Displayed Data Row = 17_{16}

= 23_{10}

60 Hz --Same--

Figure 4.2 presents the timing of a frame showing the relationship between the Valid Character Addresses (for the 24 80-character rows) and the Blanking and Sync signals. The left and right edges correspond to the start of Horizontal Sync, and the top and bottom edges (different for 50 Hz and 60 Hz) correspond to the start of Vertical Sync. The inner solid-lined rectangle (24 Data Rows x 80 characters) represents the time during which the CRT Chip outputs valid addresses on H6→HØ (A23-32→38, page 4), R3→RØ (A23-4,5,7,8), and DR4→DRØ (A23-30,29,28,27,26). The H6→HØ lines go from Ø to 79 on each scan across the 80 character positions. R3→RØ count out the 24 character rows, covering all rows Ø through 23 on each frame (the starting and ending counts are programmatically changed using the Last Data

FIGURE 5.2: CRT CHIP TIMING
(See Section 5.4 for final video timing.)



Row Control and/or the Up Scroll command).

The positive-true blanking signal (BL, A23-17, page 4) is emitted 1 character time after the end of the last (80th) character to the end of the 1st character address, as well as continuously from the end of the last character row until the beginning of the first character row. (Note that additional data pipelining and blanking flipflop delays cause the final video and blanking to have a different timing relationship--see Section 5.4.)

The Horizontal Sync (HSYN, A23-15) and Composite Sync (CSYN, A23-10) are each delayed by 1 character time (as for blanking, above) and additionally have a "front porch" of 3 more character times before the HSYNC begins. (See Section 5.4 for final video/sync/blanking relationships.) The HSYN signal and the horizontal part of CSYN are 8 character times long.

Vertical Sync (VSYN, A23-11, page 4) starts after the last scan line of the frame and lasts for 3 horizontal scan line times. CSYN is VSYN OR'd internally with HSYN. The programming of the Total Scan Lines per Frame determines whether there are 50 or 60 frames per second. Following the last scan line (at the same time VSYN starts) the Vertical Data Start is delayed by 50 scan lines for 50 Hz and by 23 scan lines for 60 Hz. This is varied to provide for approximately the same vertical centering for both 50 Hz and 60 Hz.

The cursor signal (CRV, A23-16, page 4) is not delayed (internal to the CRT Chip) and is emitted during the times when the internal Cursor Address matches the Character Address (row (DR5→DRØ) and horizontal position (H6→HØ)). (Note that the external pipeline and delays will cause the final video and cursor to have the same relationship but actual displayed video occurs two character times later; see Section 5.4).

Refer to the CRT Chip Specification (Appendix B) for the functional operation of the other (non-initializing) CRT commands. Section 2.4.1 provides the I/O addresses to be used for these commands. (Note that Processor Self Load and Non-Processor Self Load commands do not apply to this system--self load is not used.)

5.3 DISPLAY RAM AND CHARACTER GENERATION

The displayed characters are stored and retrieved from the 2114-3 RAMs (random access, read/write memories) shown on page 3. There are two display pages (banks) of 1920 characters (bytes) each. Display Page 1 is composed of A6,8,10 and 12 and is enabled when +PG SEL (A47-2, page 1) is low (logic Ø). (+PG SEL is data bit Ø on output port 4ØCH. See Section 2.4.1.) +PG SEL enters the decoder 74LS139 (A27-3, page 3) to cause the proper RAMs to be selected, as described in this table:

TABLE 5.1: DISPLAY RAM CHIP SELECT

	DISPLAY PAGE 1		DISPLAY PAGE 2	
+PG SEL	0	0	1	1
HIGH ORDER ADDRESS BIT (A10 or +RAM1Ø)	0	1	0	1
RAM Chip for +DISP DATA 7,2,1,Ø (IC Numbers are given.)	A12	A10	A9	A11
RAM Chip for +DISP DATA 6,5,4,3 (IC Numbers are given.)	A8	A6	A5	A7

The 11 address lines come from either of two sources: the CPU's +AØ→A1Ø or from the CRT Chip (and associated logic) addresses +RAMØ→+RAM1Ø. The CPU's address lines are the normal ones (as described in Section 2.2.2). The CRT Chip's address lines are derived from the data row (DRØ→4) and data column (HØ→6) address outputs (see A23, page 4). Combinatorial logic gates (page 4;

A34-1,2,3, A34-11,12,13, A37, A38-1,2, A38-3,4, A38-5,6, and A38-8,9) condition the CRT address outputs such that:

(1) the 1st 64 characters of each data row are ordered sequentially in the +RAMx addresses from Ø to DFFH.

(2) the last 16 characters of each data row are placed in the +RAMx addresses from EØØH to FFFH (with 8 16-byte holes being unused).

Table 2.1 in Section 2.3.3 shows exactly which +RAMx addresses correspond to the character position addresses. This mapping is performed in order to get the 1920 characters within the 2048-byte RAM, by transforming the 12 row/column addresses (5 row, 7 column) into 11 RAM address lines.

The most significant address bit (1Ø) enters the same decoder (page 3, A27-2), as did +PG SEL. Table 5.1, above, shows how this selects a pair of RAM chips.

The selection between the CPU addresses (+AØ→+A10) and the CRT chip's refresh addresses (+RAMØ→+RAM1Ø) is made using three quad multiplexers (A24, A25, and A26, page 3). The multiplexers normally select the CRT Chip addresses, but when the CPU performs an external data read or write with +A11 = 1 then the multiplexers automatically select the CPU's address lines. The advanced read-or-write signal +ADVRDOR WR (from A39-6, page 1) is gated with +A11 (at A40-1,2,3, page 3) to form the multiplexer control signal.

Data between the CPU (via +DB7→Ø) and the display RAMs (+DISP DATA 7→Ø) is transferred through the 8304 bi-directional transceiver (A13, page 3). The +RD PULSE from the CPU (A38-12 inverted from A54-8, page 1) controls the direction of the transceiver for CPU reads from or writes to the RAM. The

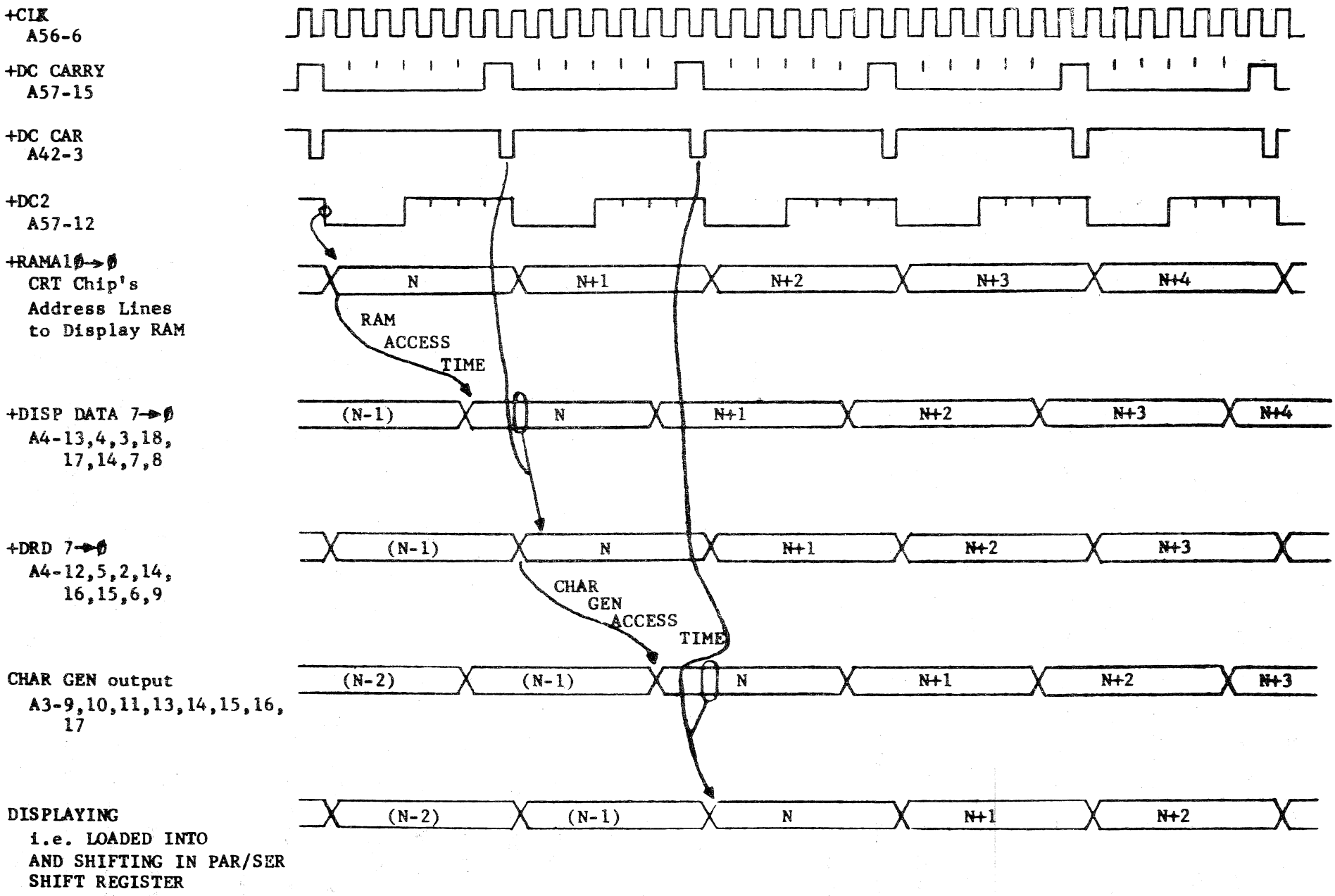


FIGURE 5.3: DISPLAY DATA TIMING

delayed read-or-write signal +RD OR WRT (A41-10, page 1) is gated with +A11 (A40-11,12,13, page 3) such that when +A11 = 1 for a +RD OR WRT the transceiver is enabled (A13-9, page 3). The delayed write pulse (-WRT PULSE, A40-8, page 1) is gated with the inverse of +A11 (A40-6, page 3) using a 74LS32 gate (A34-8,9,10) to generate the write-enable signal that goes to the RAM's. (pins 10). This signal is delayed by -WRT PULSE) at the beginning to provide proper address setup time, but goes away early (with the CPU's -WR signal) to provide guaranteed data (on writes) and address hold times.

The CPU can synchronize itself with the video so that it only accesses during blanking periods. The synchronization can be done such that one character can be transferred during horizontal blanking by using -ADV BLANK which is connected to T1 (A54-39, page 1); or the CPU can transfer a number of characters during vertical blanking by reacting to -VSYNC which is connected to INT (A54-6, page 1). Failure to synchronize may cause 1 or 2 displayed character's worth of a scan line to be garbaged on the CRT. This might appear as "drop-outs" on the display.

During normal display refresh cycles the addresses to the RAM's are multiplexed to come from the CRT chip's +RAMØ→1Ø. (+PG SEL is still in effect, see Table 5.1). The data being read from the RAMs on +DISP DATA 7→Ø goes to the pipeline latch (A4, page 5). Figure 5.3 shows the timing for accessing and transferring the display data. +DC CAR (A42-3, page 5) shows the times for accessing or transferring successive characters. +DC2 is the basic data character clock going to the CRT Chip (being inverted and input or DCC, A23-12, page 4).

The +RAM A1Ø→Ø addresses from the CRT chip change following the indicated edge of +DC2. Call this new address "N". The RAMs access location N,

putting valid data onto the +DISP DATA 7→Ø lines before the next +DC CAR pulse. When that pulse occurs the +DISP DATA for character N is loaded into the pipeline latch (A4-11, page 5) causing the outputs of the latch (+DRD 7→Ø) to be the code for character N. (Refer to Figure 5.3.)

+DRD 6→Ø comprise part of the address inputs to the character generator ROM. Three of the scan row address lines +DOTA 2→Ø (A23-5,7,8) provide the rest of the address inputs. (DOTA 2→Ø do not change on a character by character basis, only line by line; see Appendix B.) During the next character-time the character generator is accessing the dot information for the addressed character's addressed scan-row, see Figure 5.3. By the next +DC CAR pulse the character generator output is available to be loaded into the shift register (A2, page 5) and the dot-shift control logic (A45, page 5, see Section 5.4). Note that while character N is being displayed, character N+2 is being accessed by the display RAM and that character N+1 is being accessed by the character generator ROM.

+DRD7 (A4-12, page 5) from the pipeline latch, indicating a character to be displayed with "half" intensity, goes to a flip-flop (A16-12, page 5) where it is latch by the next +DC CAR. This causes the displayed character's video intensity to be reduced (see Section 5.4). The pipeline latch outputs +DRD5 and +DRD6, when both low, cause the video to be suppressed and +DRD4,3, 2,1, and Ø to be used as special control information. Section 5.4 describes the operation of these circuits.

The character generator is designed to produce patterns for 96 characters. (32 character positions are lost for the control codes referred to above.) Each character has 8 scan lines available and 8 bits of pattern information

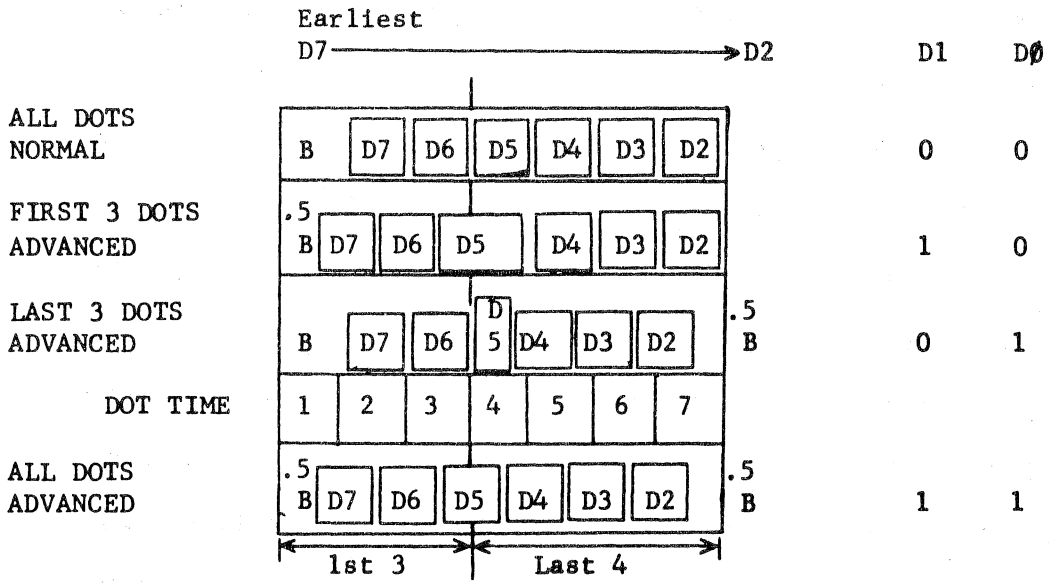
are produced. This calls for a ROM capacity of 128 (=96+32) characters X 8 scan lines X 8 bits = 8K bits. The ROM's socket location is made to accept a 2758, 2716, or 2316E. The 2758, being exactly 8K bits, satisfies the requirements. To use it jumper W30 (page 5) must be installed and switch S2,19 (page 5) must be closed. The 2716 and 2316E, being 16K bits, have twice the capacity and can provide two different character sets. S2 closed provides one and S2 open provides the other. (Jumper W30 must always be installed.)

There are 10 raster scan lines (Ø→9) per character row, but only 8 can have specified display data in the character generator. Rows Ø and 9 are always blanked as far as pattern information from the character generator is concerned (but row 9 may have the controlled underline information, see Section 5.4.). This is why only three scan line addresses, enter the character generator ROM (A3-6,7,8 page 5). Each consecutive 8 locations in the ROM are for each character. Note that the first 32 characters (groups of 8) are lost, as described above. Location Ø within a group of 8 for a character, has the video pattern information for the rastor scan line number 8 (out of the Ø→9). The locations 1 to 7 have information for scan line number 1 to 7, respectively. For example the character at locations 1ØØH to 1Ø8H (the first displayable character, i.e. the 33rd group of 8) has the following relationships:

1ØØH	Scan Line 8 data pattern
1Ø1H	" " 1 " "
1Ø2H	" " 2 " "
1Ø3H	" " 3 " "
1Ø4H	" " 4 " "
1Ø5H	" " 5 " "
1Ø6H	" " 6 " "
1Ø7H	" " 7 " "

The data pattern for each scan line of each character is determined from the 8 bits at the ROM location. 6 of the bits represent the actual dots to be displayed. The other 2 bits specify the half-dot shift characteristics of the 6 displayed bits. This half-dot shift characteristic provides for a much finer horizontal resolution without increasing CRT bandwidth requirements. ROM output bits D1 and DØ (A3-10,9, page 5) provide the dot shift specification. D7→D2 (A3-17,16,15,14,13,11) provide the actual dot information. D7 goes out first in time. A 1 for any bit indicates positive (brighter) video. The 4 possible half-dot shift patterns are as follows:

FIGURE 5.4: DOT SHIFT FORMATS



B = Blank Dot Position
.5B = ½ Blank Dot Position

NOTE: The dots and shift controls must be encoded such that there will be no ½ dot actually formed (i.e. ½-dot on or off between two other dots that are both the same but opposite the polarity of the ½-dot).

Section 5.4 describes the operation of the video generation circuitry that displays the above-described character patterns.

5.4 VIDEO GENERATION

Basic Video: The basic video "dots" (1) emanate from the shift register A2-13, page 5) (2) are then delayed by either one full or one-half dot time (A17-5 or 9, respectively) with the desired one being selected (using A18-1,2,3 and A18-4,5,6 along with the two inputs A19-2,4 and output on A19-6), (3) are next complemented if dictated by controls and/or +CURSOR (A21-4,5,6), (4) are then open-collector driven onto a multi-level video point where there is blank, half, and full intensity and, possibly, sync levels (video is driven by A15-4,5,6), and (5) are finally emitter-follower driven onto P2-4 (by Q1, page 5).

SHIFT REGISTER: The character generator's 6 output pattern bits are loaded into the shift register as shown in Figure 5.3. +DC CARRY (A57-15, page 4) causes the load (via A42-11,12,13 to A2-15, page 5) at +CLK rising. This load may be inhibited (at A42-13, page 5) by a number of conditions (at A19-8, 9,10,12,13, page 5). These inhibit conditions are:

(a) control character code (+DRD5 = Ø and +DRD6 = Ø), as detected by A22-1,2,3 which goes to A19-13.

(b) first scan line for a character row (+DOT. A3→Ø = ØØØØ) as detected by A22-8,9,10, A21-11,12,13, and A22-4,5,6 which go to A19-9.

(c) control registers say flash (A31-5 = 1 and A31-9 = 1, page 5) and +4Hz divided-by-2 (A34-5) equals Ø, as detected by A33-3,4,5,6 which goes to A19-10.

(d) tenth scan line for a character row (+DOTA3→Ø = 1ØØ1) as detected by A20-11,12,13 which goes to A19-12.

The above inhibiting conditions (at A19-8, page 5) are also loaded into the flip flop A16-2,6 (page 5) with the +DCCAR pulse. The flip flop's

output clears the shift registers contents during the first dot time. (See Figure 5.5.)

Normally (when allowed to load) the 6 data bits (from D7→Ø of the character generator) are shifted as shown in Figure 5.5. For the 7th dot time a Ø emanates from the shift register (QH, A2-13, page 5). All bits are shifted into the two dot select flip-flops (A17-9,12 and A17-2,5) where one (A17-9,12) is clocked by -CLK (at A17-11), allowing that flip-flop to have the data from the shift register in advance of the other normally clocked flip-flops (A17-2,5). This means that A17-9 has the "advanced" dot and A17-5 has the "normal" dot.

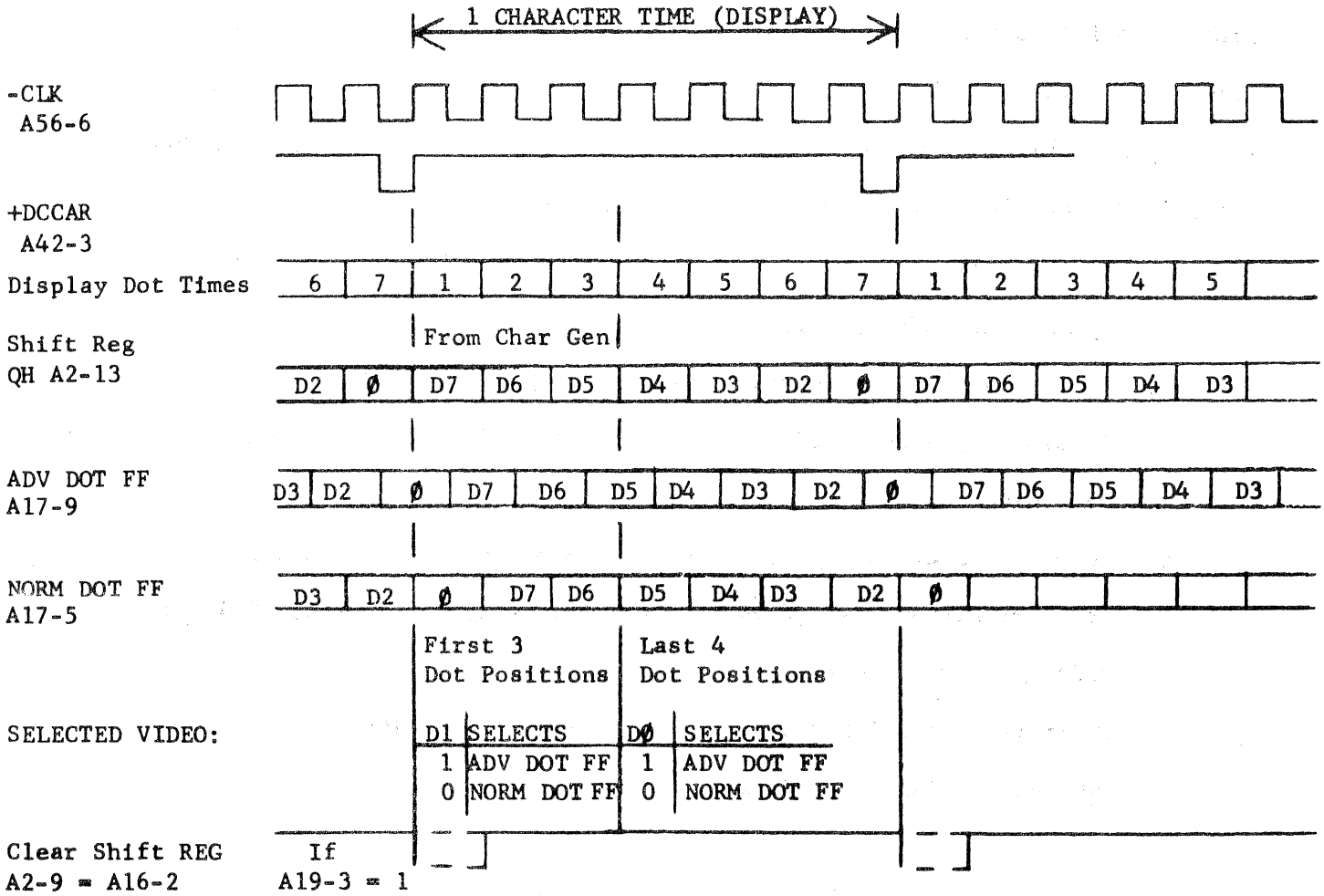


FIGURE 5.5: VIDEO DOT

DISPLAY SIGNAL RELATIONSHIPS (VIDEO, BLANK, CURSOR, HSYNC): The relationships between the various signals that directly effect the display are shown in Figure 5.6. The top portion of the diagram has the relative character positions for the "display RAM", "character generation", and "displaying video" activities. (See Figure 5.3 for more details.) Shown in Figure 5.6 are the first few and last few character positions for a horizontal scan line.

The following signals are controlled by CRT outputs:

(1) RAM Accessing (display RAM address for indicated character)

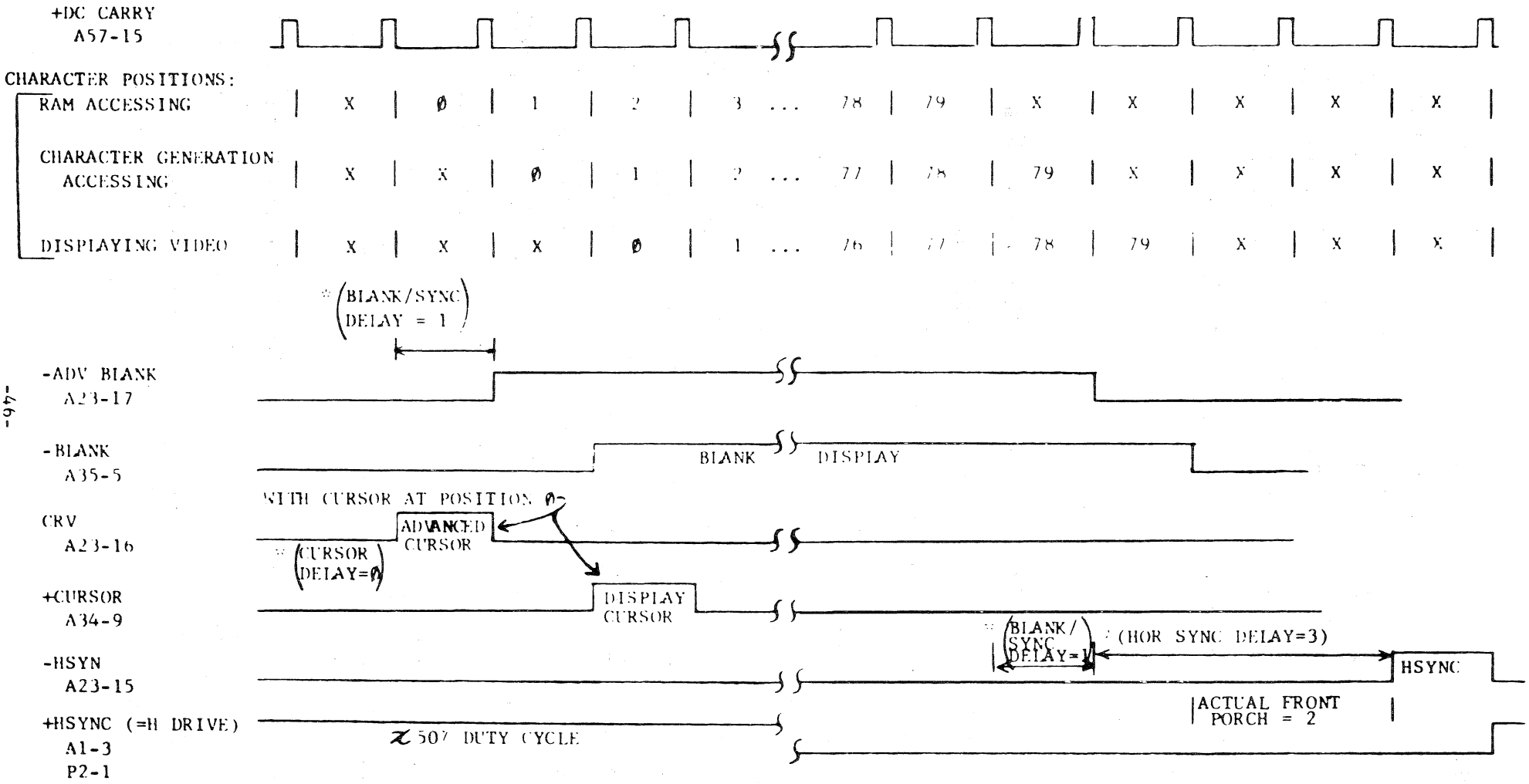
(2) -ADV BLANK (delay by 1 with respect to addresses)

(3) CRV (delayed by Ø with respect to addresses)

(4) HSYN (delayed by 1 with respect to addresses)

The delays are as programmed into the CRT chip, see Section 5.2. -ADV BLANK is delayed one more character time (by A35-2,5, page 4, as clocked by +DCCAR) in order to line it up with displaying video. This +BLANK signal (A35-5) goes through an open collector driver (A14-12,13, page 5) in order to blank the video. ADV BLANK and BLANK are used for addition gating functions as described in other parts of this section. Additionally, -ADVBLANK goes to the CPU's T1 input (A54-39, page 1) to permit synchronization with the video by the CPU for performing accesses to the display RAM without disturbing the display refresh. (See Section 5.3.)

The cursor signal from the CRT Chip (A23-16, page 4) is delayed 2 character times (by A35-9,12 and A34-1,12, clocked by +DCCAR, page 5) to line it up with the video being displayed. The +CURSOR signal complements the normal video signal (using A21-1,2,3 and A21-4,5,6, page 5) including the effect



*See Section 5.2 for CRT programming.
NOTE: See Figure 5.3 for character position details.

FIGURE 5.6: DISPLAYED VIDEO RELATIONSHIPS

of the INVERT VIDEO bit (A28-6 to A21-2) of the control register. Additional gating (at A18-11,12,13, page 5) permits optional (by installing jumper W25) 4 Hz flashing (on-off) of the video at the cursor position. For this option when the cursor is flashing "on" (A18-11=Ø), the Zero-Intensity driver (A15-1,2,3, page 5) is disabled and "on" video is injected into the video signal (at A19-1, page 5). During Zero-Intensity this causes video to be "on" (not because of the injected "on" video but because the Zero-Intensity signal, A32-6, disables the video driver, A15-4, 5,6, through an inverter, A33-1,2,12,13). During other (non-zero) intensities the cursor "on" causes the character position to have all dots "on" because of the injected "on" video. This causes the character's background to change (flash) to the same polarity as the character itself (which is already inverted once or twice by the +CURSOR signal and, possibly, by the INVERT VIDEO control bit).

Horizontal sync (A23-15, page) is programmatically delayed in the CRT Chip by 4 character times (1 for SYNC/BLANK DELAY and 3 for HSYN DELAY, see Section 5.2) from the end of the last RAM address character position. With video being delayed 2 more character times a 2-character "front porch" is provided (see Figure 5.6 and Appendix B). HSYN (A23-15) is inverted (A36-10,11, page 4) to drive a one-shot (A1-2,3) which generates a horizontal drive signal (called +HSYNC) that goes to the video connector (P2-1, page 5). (-HSYNC is also used for other timing (on page 5) as described in the paragraph below that presents the video control register.)

VSYNC (A23-11, page 4), which is inverted twice (A56-12,13 and A56-1,2, page 4) and driven (by A14-10,11, page 5) onto -VSYNC (P2-5), has the timing as described in Section 5.2 and Appendix B. (VSYNC signals are

also used for video control register timing, see below.) -COMPSYNC (A23-10, page 4) is inverted (A15-11,12,13, page 5) and driven (by inverting driver A14-8,9, page 5) onto P2-6. Its main use is to provide the composite sync to the multi-level video signal (by closing switch S2-10,11 and opening switch S2-1,20, page 5). When the switch settings are made then P2-6 provides +TTL VIDEO in addition to a TTL composite sync signal.

HALF-DOT-SHIFT LOGIC: As described in Section 5.3 each scan line of each character can specify a half dot shift characteristic for each the first 3 dot positions and the last 4 dot positions. D1 (from A3-10, page 5) selects the half dot shift for the first 3 dot positions (D1=1 selects the advance dots, D1=Ø selects normal dots. DØ (A3-9) selects the half dot shift for the last 4 dot positions. Section 5.3 shows a portrayal of the 4 possibilities. D1 and DØ are latched into A45-2,5 and A45-12,9 (respectively) by +DCCAR (A42-3 to A45-3 and A45-11) which is the same time as when the shift register is loaded. The outputs of A45-5,6 determine whether the normal or advanced dot is selected. The Q output (A45-5) enables (via A18-4,5,6) the advanced dot (from A17-9). The $\overline{Q}$ output (A17-6) enables (via A18-1,2,3) the normal dot (from A17-5). +DC2=1 and +DCØ=Ø (inverted by A44-12,13, page 5) cause (via A46-3,4,5,6 and A46-8,9, 10,11) the selecting flip-flop A45-2,5) to take on the value of the flip-flop that stored the DØ value A45-9,12). This occurs between the 3rd and 4th dot time (see Figure 5.1) causing the dot shift patterns shown in Figure 5.4. The dot-select gates (A18-4,5,6 and A18-1,2,3) have their outputs OR'd (with other signals at A19-2,4) to form the pre-complemented video signal at A19-6.

IN-STREAM VIDEO CONTROL REGISTER: Six flip-flops implement a 4-bit control register that captures video control information from the display character

stream. As described in Section 5.3 the control information comes from the outputs of the pipeline latch (A4, page 5) and uses up 32 (of the possible 128) character encodings. A control character is denoted by having bits 6 and 5 equal to Ø (+DRD6 and +DRD5, A4-5,2) which is detected by the gate A22-1,2,3, page 5. The output of this gate (A22-3) is inverted (A44-1,2) to yield +CONTROL. The control register flip-flops are clocked by signals that are essentially the same as +DCCAR (see Figures 5.3 and 5.5) but are enabled only under the following conditions:

(1) +CONTROL is true;

(2) valid characters are in the character stream at the pipeline register A4 (which is when the signal -ADVBLANK is high, see Figure 5.6);

(3) the intensity control bits (+DRD3,2) require that +DRD4=1 to be clocked.

These conditions are gated (using A43-12,3, A43-4,5,6, A43-8,9,10, A42-4,5,6, and A42-8,9,10, all on page 5) with +DCCARRY (at A43-5) and -CLK (at A42-4 and A42-10) to generate the clocking signals for the UNDERLINE (+DRDØ) and INVERT VIDEO (+DRD1) bits (as clocked from A42-6) and the INTENSITY bits (+DRD3,2, as clocked from A42-8 which is inverted by A44-10,11, page 5).

CONTROL CODES: BIT 6=Ø, BIT 5=Ø

THEN START UNDERLINE BIT Ø=1

END UNDERLINE BIT Ø=Ø

START INVERSE VIDEO BIT 1=1

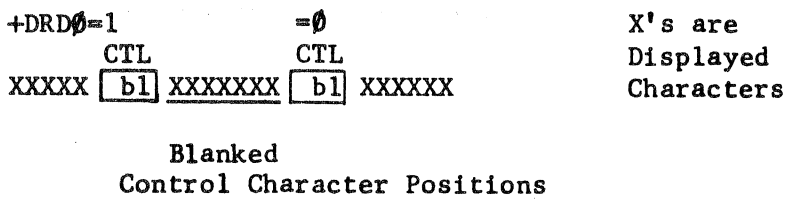
END INVERSE VIDEO BIT 1=Ø

IF ALSO BIT 4=1 THEN

	BIT 3	2
START ZERO INTENSITY	Ø	Ø
START FLASH (2Hz)	1	1

	BIT 3	2
NORMAL	1	Ø
NORMAL	Ø	1

UNDERLINING: Bit Ø of control characters (+DRDØ, A4-9) is clocked (A29-11) into the UNDERLINE flip-flop (A29-9,12, page 5). If +DRDØ = 1, then, to prevent the control character position itself (which is blanked, as described in the "SHIFT-REGISTER" paragraph above) from being underlined, a second flip-flop (A28-9,12) provides a one-character delay. The second flip-flop is clocked by +DCCAR at every character time. If +DRDØ=Ø, then the output of the first flip-flop (A29-9) clears the second immediately (via A28-13), causing the underline to disappear at the beginning of a control character:



The actual underlining (as controlled by A28-9) is gated (at A18-8,9,10, page 5) with +10th Dot Row which indicates the last rastor scan line for a character row (as denoted by A20-11,12,13 and inverted by A80-1,2,3, page 5). The output of the gate (A18-8) forces a video "on" condition (at A19-5). (See also Inter-Scan-Line Storage, below.)

INVERTED VIDEO: Bit 1 of control characters (+DR01, A4-6) are clocked (A29-3) into the INVERTED VIDEO flip-flop (A29-2,5, page 5). As with the UNDERLINE flip-flop pair (described above), the INVERTED VIDEO has two flip-flops (A29-2,5, and A28-2,5) which, when Bit 1=1, delay the effect on the video until the following character, but when Bit 1=Ø they turn off the inverse video immediately (using the second flip-flop's clear,

A28-1). The actual inverting (as controlled by A28-6) is exclusive OR'd with the +CURSOR signal (at A21-1,2,3, page 5) and the video signal (using A21-4,5,6). Thus the video may, in effect, be complemented twice, once by the INVERT VIDEO control and once by the +CURSOR signal. If the flashing cursor option (jumper W25) is not installed then the presence of the cursor at the end of an INVERT VIDEO field will cause ambiguity in visually determining the cursor position on the screen. (See also Inter-Scan-Line Storage, below.)

INTENSITY CONTROLS: When bit 4 (+DRD4, A4-14) of control characters equals 1, then bits 3 and 2 (+DRD3,2, A4-16,15) are clocked (A31-3,11) into the INTENSITY control flip-flops (A31-2,5 and A31-9,12, page 5). These flip-flops affect the intensity immediately when loaded. When bit 3 (A31-5) and bit 2 (A31-9) both equal zero, this is detected (by gating A31-6 and A31-10 at A32-4,5,6, page 5) and causes a driver (A15-1,2,3) to zero the video. (This driver may be disabled at the cursor position at a 4 Hz on-off rate, if the flash cursor option, jumper W25, is installed. See CURSOR, above.) When bit 3 and bit 2 both equal one, this is detected and gated with a 2 Hz square ware (at A33-3,4,5,6, page 5) in order to produce a video flashing (on-off) effect. The gate's output (A33-6) inhibits and clears the dot shift register (via A19-10,8). (See SHIFT REGISTER, above.) Any other combinations of bits 3 and 2 (specifically bit 3,2, = 1,0 or = Ø,1) allow the normal intensity to be used.

INTER-SCAN-LINE STORAGE OF CONTROL REGISTER: The register A30 (page 5) stores the CONTROL REGISTER values at the end of the 80th character at the 10th scan line of a character row. At the beginning of each of the 10 scan

lines of the next character row the values in the storage register are loaded into the control register flip-flops. This allows UNDERLINE, INVERTED VIDEO, and INTENSITY controls to carry over from one character row to the next character row. The storage register (A30) is loaded at the end of the tenth scan line by gating -BLANK, +ADVBLANK, and +10th DOT ROW (all at A33-8,9,10,11, page 5) which, when all equal to 1, define that the 80th character on scan line 10 is being displayed. The gate's output (A33-8) passes through A32-9,8 to provide one of the load enables for the storage register (A30-9). The other load enable (A30-10) is driven true by -10th DOT ROW (A20-11 through A32-11,12,13). In this way the storage register is loaded with the control register bits -BITØ (from A29-8), -BIT 1 (A29-6), -BIT 2 (A31-10, and +BIT 3 (A31-5) into storage register data input 4D, 3D, 2D, and 1D (A30-11,12,13,14), respectively.

Before loading the control register flip-flops at the beginning of each scan line, all flip-flops are set to their initialized condition by the -HSYNC (A36-10, page 4) signal:

UNDERLINE (A29-9) is set to Ø (via A29-13)

INVERT VIDEO (A29-5) is set to Ø (via A29-1)

INTENSITY (bits 3,2 at A31-5,9) is set to 1,Ø (via A31-4,13)

The outputs of the storage register are enabled (A30-2) by the combination of +ADV BLANK and +BLANK (at A20-4,5,6) (except during VSYNC, see below). These outputs go to the 4 control flip-flops causing them to preset or clear in a manner appropriate with the stored bit value. If a stored bit is high at the output then the corresponding flip-flop is not changed because the "initialized state" (see above) is already correct. If a stored bit is low

at the output then the flip-flop is forced to the opposite of the "initialized state". The flip-flops end up in the state indicated by the storage register:

NAME	BIT #	INITIALIZED VALUE	STORAGE REGISTER VALUE	FINAL FLIP-FLOP VALUE
UNDERLINE	Ø	Ø	(= -BITØ) Ø	1
			1	Ø
INVERT VIDEO	1	Ø	(= -BIT1) Ø	1
			1	Ø
INTENSITY	2	Ø	(= -BIT2) Ø	1
	3	1	(= +BIT3) Ø	Ø
			1	1

Figure 5.7 Storage Register Value

Additionally, during vertical blanking, the signal -VSYNC (A36-12, page 4) causes (through A32-8,9,10 and A32-11,12,13) both enables (A30-9,10) of the storage register be driven true. +VSYNC (A36-2) forces the storage register's outputs to be disabled (at A30-1). This causes the control flip-flops to stay in their initialized state as forced by -HSYNC (from A36-10, page 4, to A29-1, A29-13, A31-4, and A31-13, page 5). This also causes the storage register to have the same values. Following VSYNC these values are:

UNDERLINE = Ø

INVERT VIDEO = Ø

INTENSITY = 1,Ø (i.e., NORMAL)

HALF-INTENSITY (="PROTECTED" by firmware): Bit 7 of every character (A4-12, +DRD7, page 5) controls whether or not that character is displayed with half intensity. At the same time the shift register is loaded +DCCAR (A42-3, page 5) loads (A16-11, page 5) +DRD7 (A16-7) in a flip-flop whose output (A16-9) is driven (by A15-8,9,10) through 510 ohms (R9) to the combined video

node. With the driver's output (A15-8) low the combined video is loaded down more, causing the intensity level, if any, to be reduced.

COMBINED VIDEO: The following open-collector drivers make up the combined video signal (A15-6, page 5):

Half intensity	A15-8 through 510 ohm, R9
Zero intensity	A15-3
Video (Dots)	A15-6
BLANK	A14-12
FORCE BLANK	A14-2

+FORCE BLANK's driver (A14-1,2) allows the CPU to blank the screen at any time (to avoid unsightly display effects, for example, during massive display data accesses). The CPU writes a 1 in bit 5 to external data (memory mapped I/O) address 40CH to cause the screen to blank. (See Section 2.4.1.)

For video without sync signals switch S2-1,20 is opened and switch S2-10,11 is closed. Resistors R2 and R3 (510 ohms and 1K ohm) provide the level pullup capability. The emitter-follower implementation of Q1 provides a high input impedance and a low output impedance which drives (through R4, 68 ohms) +VIDEO (P2-4). A convenient ground signal is provided on P2-3.

For composite video (i.e., video with sync signals) switch S2-1,20 is closed and switch S2-10,11 is opened. This puts a 260 ohm resistor (R1) in series with the previous combined video which prevents zero intensity from reaching as low a level at S2-1. Closing S2-1,20 allows composite sync (A14-8) to cause the lowest level in the new video signal. This "TTL" driven video signal is output on P2-6 +TTL VIDEO. As above, the signal is driven by the emitter follower (Q1) to drive +VIDEO (P2-4).

6. COMMUNICATION OPERATION

6.1 Baud Rate Generation

The baud rate frequencies for the computer (P3) and printer (P4) serial communication interfaces are determined by the counters and switches shown on page 6 of the schematics. The input clock is TDC1 (A57-13, page 4), which is an asymmetrical 3.402 MHz signal (see Figure 5.0). The first counter (A73, page 6) divides this by 11 to yield a 309,273 Hz signal (A73-11) suitable for the 19,200 baud rate. Counter A70 and A71 each provide 4 levels of dividing by 2 to yield clocks for 9600 down to 75 baud. Counter A72 divides A70's output by 11 to yield (at A72-11) a clock suitable for 110 baud.

Switch S1 selects the baud rate for the computer (P3) port by enabling one (and only one, as enforced by the user) signal to A74-9 (page 6). (See Section 3's table for switch settings.) Switch S3 does the same for the printer (P4) port by enabling one signal to A74-2. The CPU selects one of these two signals with +SELLPT (A74-1,2,3) the printer port and -SELLPT=1 enables (at A74-8,9,10) the computer port. +SELLPT is controlled by the CPU as bit 4 in memory mapped I/O port 40CH. (See Section 2,4.1.) The selected baud rate results in +BAUD GEN (A47-11,12,13) which goes to the UART (A48-12,40, page 2).

6.2 UART Operation

Details of the UART chip's (A48, page 2) internal operation are given in its specification in Appendix C. Section 2.4.2 presents programmer-level I/O information.

UART I/O Interface: Three I/O ports (2 read and 1 write) are used to interface the CPU to the UART. The data write port (address 408-H) is enabled by address decoder output 2 (A58-3, page 1) which goes to the UART's - DS (A48-23, page 2). When pulsed (as per Section 2) on this input the UART receives a byte on CPU data lines (+DB7→Ø) which are connected to UART inputs DB8→Ø (page 2). The data read pulse, -RDE (address 408H), from the decoder (A58-6) enables (RDE, A48-4) the UART's read outputs (RD8→L) onto the CPU data bus (+DB7→Ø, respectively). -RDE also pulsed the UART's reset Data available input (A48-18). The status word enable read pulse, -SWE (address 404H), from the decoder (A58-7) enables (48-10) four status bits onto the CPU data bus:

FE, Frame Error,	from A48-14 to +DB3
PE, Parity Error,	from A48-13 to +DB2
TBMT, Transmit Buffer Empty,	from A48-22 to +DB1
DTA, Data Available,	from A48-19 to +DBØ.

UART SWITCH CONTROLS: Five switches provide operational control over the UART, see Appendix C and Section 3:

S2-5, 16	Parity	A48-35
S2-6, 15	Stop Bits	A48-36
S2-7, 14	Number of Bits	A48-38
S2-8, 13	" " "	A48-37
S2-9, 12	ODD/EVEN PARITY	A48-39

The -HALF DUPLEX signal goes directly into the CPU (A54-38, page 18, from switch S2-3,18). It is not implemented with the UART, but by the firmware.

UART RESET: The CPU resets the UART by pulsing the -PROG pin (A54-25, page 1) which is inverted (by A67-1,2, page 1) yielding +RESETUART to drive the UART's MR input (A48-21, page 2).

UART SERIAL OPERATION: As described in Appendix C the UART uses the receive and transmit clocks, (A48-17,40) at 16 times the baud rate, to transmit data (A48-25) and receive data (A48-20). The clock is as selected in the BAUD RATE GENERATION logic (+BAUDGEN, A74-11, page 6; see Section 6.1).

6.3 SERIAL INTERFACES

The computer and printer serial interfaces can be either RS232C-type levels or current loop. The serial data is transmitted as both RS232 and current loop (for the selected interface). Two switches must be set to select which type of data will be received on the computer port:

Receive RS232C on P3-3 -- Close S5-6,9

Receive Current Loop on P3-12,24 -- Close S5-7,8

(only one switch should be closed).

6.3.1 RS232 Operation:

COMPUTER PORT, P3:

Receive Data is input on P3-3 (by A60-12, page 2) and passed through switch S5-6,9 to the UART (A48-20). (See also Section 6.3.3 for P6).

Clear to send is input on P3-5 (by A60-8,10) yielding -CTS which the CPU can input on TØ (A54-1, page 1). (See also Section 6.3.3.)

A "Data Carrier Ready" signal can be selectively input on P3-6 (as switched by S5-1,14) or on P3-8 (as switched by S5-2,13). With both switches open 3.3KΩ resistor (R32) pulls the input to +12V, the true condition. The output of the RS232 receiver (A60-11, page 2) becomes -DCR which the CPU can read on port 2 bit 5 (45-36, page 1). (See also Section 6.3.3.)

Transmit Data for the computer RS232 port is driven to P3-2, TXD, (by A59-4,5,6, page 2). The input to the driver (A59-4,5) is enabled (at A61-4,5,6) by the control signal -SELLPT (A62-4 to A61-5) which, before inversion (by A62-3,4), is +SELLPT as output by the CPU on bit 4 of memory mapped I/O port 40CH (See Section 2.4.1). When -SELLPT disables the transmit port (-SELLPT low) the output (at A59-6, P3-2) is kept low (defined by the RS232C specification as the "OFF", marking condition, or binary 1 condition.) -BREAK (A47-10, page 1, CPU output to 40CH bit 3) when true (low) can force (via A61-11,12,13, page 2) the transmit data to the spacing condition (RS232 is positive, defined as "ON") if enabled (at A61-4,5,6) by -SELLPT being high. The data signal itself (at A61-12) comes from the UART's -TXD output (A48-25). (See also Section 6.3.3 for P6.)

The CPU controlled -RQS signal (A47-7, page 1, CPU output to 40CH bit 2) is the source for driving (using A59-2,3, page 2) the RTS signal at P3-4. By closing switch S5-3,12 this driver will also drive DTR at P3-20. Alternatively, DTR could be pulled permanently to the "ON" (positive) state by closing switch S5-4,11 (and leaving S5-3,12 open).

Pin P3-7 is ground on the RS232 computer port.

PRINTER PORT, P4:

The RS232 printer port has no serial data receive capability. However +PRTRDY (P4-20, page 2) is received (by A60-4,6) and sent to the CPU as -PRTRDY (A60-6, page 2) on CPU port 2 bit 6 (A54-37, page 1). If P4-20 is left disconnected, then a 3.3KΩ resistor (R18) pulls the signal to the ON state.

Transmit Data for the printer RS232 port is driven to P4-3, PRT DATA (by A59-8,9,10, page 2). The input to the driver (A59-9,10) is enabled (at A61-8,9,10) by the control signal +SELLPT (A47-12, page 1) which is output by the CPU on bit 4 of output location 40CH (See Section 2.4.1). The transmit data is otherwise controlled by +SELLPT and -BREAK in the same manner as described above (for -SELLPT and -BREAK) for the computer RS232 transmit data, above. The data, as above, originates from the UART's -TXD (A48-25).

The RS232 printer port also drives (with A59-11,12,13) P4-6 (by installing jumper W12) and/or P4-8 (by installing jumper W13) with the CPU controlled signal -RQS (A47-7, page 1, CPU output to 40CH bit 2).

Pin P4-7 is ground on the RS232 printer port.

6.3.2 Current Loop Operation

COMPUTER PORT, P3: The computer has both transmit and receive current loop interfaces. The receive circuit uses an opto isolator (4N37 at A6-3, page 2) to receive a current loop with current (conventional) entering at P3-12 (RXD1) and leaving at P3-24 (RXD2). Adiode (D2) provide a reverse current path. The opto-isolator's output (A63-5) feed an inverted (A62-10,11), the

output of which (when passed by a closed S5-7,8 switch) provide the UART with serial input data (A48-20). (Note that the RS232 switch S5-6,9 should be open during current loop operation). The current loop receiver circuit is very low impedance such that the equipment driving this input must limit the current, to not more than 40 mA (with a 20 mA minimum).

The current loop driver for the computer port is opto-isolated (A65,4N33) also. Its source (via A62-5,6) is the same as what is input to the RS232 driver, causing it to parallel that pin's actions (See Section 6.3.1). A completely isolated output is provided at P3-25 (TXD1) and P3-13 if jumpers W14 and W16 are installed (and jumpers W15, W17, and W6, and resistor R28 are not installed). Alternatively by installing R28, W6, W15, and W17, a current (limited by R28) can be driven into P3-25 (TXD1) and returned to ground at P3-13 (TXD2).

7. KEYBOARD OPERATION

The keyboard matrix is driven on connector P1 (pins 8 to 15) by the CPU with bits 7 to Ø of port 1 (A54-34 to 27), page 1). The twelve inputs are received by multiplexers (with all of A69 and A68-9 to 15, and 2, page 1) to be received by the CPU via the four memory-mapped input locations 4ØC, 4ØD, 4ØE, and 4ØF (Hex) as described in Section 2.4.3. This is done using the 4ØC decoder output KBRD (A58-9, page 1) and +A1 and +AØ (at A69-2,14 and A68-2,14), causing the multiplexers to output data on +DBØ (A69-9), +DB1 (A69-7), +DB5 (A68-9). Additionally for all addresses 4ØC to 4ØF separate switches from the keyboard are input on the following bits:

+DB2	P1-5	FUNC	(using A76-11,12)
+DB3	P1-6	CTL	(using A76-13,14)
+DB4	P1-4	SHFT	(using A76-2,3)
+DB5	P1-3	ALPHA	(using A76-4,5)

See also Section 2.4.3 for CPU interface usage and Appendix C for the standard keyboard matrix expected on the interface.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	K	L	E	G	H							
1	1	1	1	1	1					C2	Cap DIP Mica 10pf 100D03	2024100
2	3	3	3	3	3					C3,6,7	Cap R/L 22uf 15V	2025700
3	1	1	1	1	1					C1	Cap R/L 1uf 15V	2027901
4	47	47	47	47	47					unmarked	Cap C/D .01uf 20% 16V	2028700
5	1	4	1	1	1					C10	Cap C/D .01uf 10% 50V Y5P	2028900
6	2	2	0	0	2					C11,12	Cap C/D 330pf 50V 20%	2029100
7	1	1	1	1	1					A42	IC 74S00	2024000
8	5	5	5	5	5					A18,20,40,61.74	IC 74LS00	2024200
9	1	1	1	1	1					A15	IC 74LS03	2024400
10	1	1	1	1	1					A55	IC 74S04	2024600
11	5	5	5	5	5					A36,38,44,62,67	IC 74LS04	2024800
12	1	1	1	1	1					A14	IC 74LS05	2025000
13	2	2	2	2	2					A32,43	IC 74LS08	2025200
14	2	2	2	2	2					A33,46	IC 74LS10	2025400
15	1	1	1	1	1					A19	IC 74LS20	2025600
16	3	3	3	3	3					A22,39,66	IC 74LS32	2025800
17	1	1	1	1	1					A58	IC 74LS42	2026000
18	1	1	1	1	1					A37	IC 74LS51	2026200
19	1	1	1	1	1					A17	IC 74S74	2026400
20	8	8	7	8	8					A16,28,29,31,34,	IC 74LS74	2026600
										35,45,77		

NOTES:

TITLE
CONTROL BOARD, TVI-912/920 TERMINAL

DATE
02-01-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	K	L	E	G	H							
21	1	1	1	1	1					A21	IC 74LS86	2026800
22	1	1	1	1	1					A56	IC 74LS109	2027000
23	1	1			1					A27	IC 74LS139	2027200
24	4	4	3	4	4					A24,25,26,78	IC 74LS157	2027400
25	5	5	5	5	5					A57,70-73	IC 74LS163	2027600
26	1	1	1	1	1					A2	IC 74LS166	2027800
27	1	1	1	1	1					A30	IC 74LS173	2028000
28	2	2	2	2	2					A41,47	IC 74LS174	2028200
29	2	2	2	2	2					A68,69	IC 75LS253	2028400
30	1	1	1	1	1					A76	IC 74LS367	2028600
31	1	1	1	1	1					A51	IC 74LS373	2028800
32	1	1	1	1	1					A4	IC 74LS374	2029000
33	1	1	1	1	1					A59	IC 75188N	2029200
34	1	1	1	1	1					A60	IC 75189AN	2029400
35	1	1	0	0	1					A65	IC H11G3	2034200
36	1	1	1	1	1					A63	IC TIL117, 4N37	2029300
37	1	1	1	1	1					A3	IC 2316 ROM A3-2	2034600
38	1	1	1	1	1					A1	IC NE555	2030200
39	1	1	1	1	1					A13	IC DP8304	2030400
40	2	2	2	2	2					A52,53	IC AMD2111-4A	2030600
41	1	1	1	1	1					A48	IC 2502, AY-5-1013A	2030800

NOTES:

TITLE
CONTROL BOARD, TVI-912/920 TERMINAL

DATE
02-01-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	K	L	E	G	H							
42	1	1	1	1	1					A23	IC 5027,5037,TMS9927	2031000
43	1	1	1	1	1					A54	IC Microprocessor P8035	2031200
44	4	4	4	4	4					A6,8,10,12	IC TMS4045-25NL, 2114 300NS	2035800
45			(4)	(4)	(4)					A5,7,9,11	IC TMS 4045 Option-2nd page	
46			0	1	1					A49B	IC 8332A 32K ROM A49B	2032600
47			0	1	1					A49C	IC 8332A 32K ROM A49C	2032600
48			(1)	0	0					A49R	IC 2316 16K ROM A49R	2032200
49			(1)	0	0					A50R	IC 2316 16K ROM A50R	2032400
50	1	1									IC A49C1	2034000
51	1	1	1	1	1					S5	Dip Switch 7 Pos Top	2174200
52	1	1	(1)	1	1					S3	Dip Switch 10 Pos Top	2181000
53	2	2	2	2	2					S1,2	Dip Switch 10 Pos Side	2096800
54	2	2	(2)	2	2					P3,4	Connector RS232 R/A	2097800
55	4	4	4	4	4					XA5,7,9,11	Socket IC 18 Pin	2098400
56			1	1	1					XA49	Socket IC 24 Pin	2098401
57	3	3	1	1	1					XA50	Socket IC 24 Pin	2098401
58	3	3	2	2	2					XA23,54	Socket IC 40 Pin	2098402
59	1	1	0	0	1					XS4	Socket IC 14 Pin	2098403
60	1	1	1	1	1					X1	Cry 23.814 MHz Fundamental	2098600
61	1	1	1	1	1					P7	Plug 2 Pin	2098501
62	2	2	2	2	2					P2,5	Plug 5 Pin	2098706

NOTES:

TITLE: CONTROL BOARD, TVI-912/920 TERMINAL

DATE: 2-1-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	K	L	E	G	H							
63	1	1	1	1	1					P1	Plug 26 Pin	2098701
64	2	2	2	2	2					R4,31	Res C/F 68 Ohm 5% 1/4W	2051100
65	1	1	1	1	1					R22	Res C/F 180 Ohm 5% 1/4W	2053300
66	2	2	2	2	2					R1,19	Res C/F 270 Ohm 5% 1/4W	2051300
67	3	3	4	4	4					R11,20,29,30	Res C/F 330 Ohm 5% 1/4W	2051500
68	1	1	1	1	1					R13	Res C/F 470 Ohm 5% 1/4W	2051700
69	2	2	3	3	3					R2,14,25	Res C/F 510 Ohm 5% 1/4W	2051900
70	2	2	1	1	1					R9	Res C/F 750 Ohm 5% 1/4W	2031700
71	6	6	6	6	6					R3,5,8,10,15,16	Res C/F 1K Ohm 5% 1/4W	2052100
72			1	0	0					R34	Res C/F 1K Ohm 5% 1/4W	2052100
73	2	2	0	0	2					R41,42	Res C/F 1K Ohm 5% 1/4W	2052100
74	1	1	1	1	1					R7	Res C/F 1.2K Ohm 5% 1/4W	2031900
75	1	1	1	1	1					R12	Res C/F 1.8K Ohm 5% 1/4W	2052300
76			1	1	1					R17	Res C/F 3.3K Ohm 5% 1/4W	2052700
77	2	2	3	3	0					R18,32,33	Res C/F 3.3K Ohm 5% 1/4W	2052700
78	1	1	1	1	1					R6	Res C/F 4.7K Ohm 5% 1/4W	2053100
79	5	5	0	0	5					R36-40	Res C/F 4.7K Ohm 5% 1/4W	2053100
80		1	0	0	1					R23	Res C/F 51K Ohm 5% 1/4W	2032300
81	1									R23		2032500
82			1	1	0					R23	Res C/F 1M Ohm 5% 1/4W	2031500
83	5	5	4	4	4					RP1,2,4,6	Res Pack 1K Ohm	2040500

NOTES:

TITLE: CONTROL BOARD, TVI-912/920 TERMINAL

DATE: 2-1-83

TeleVideo Systems, Inc.

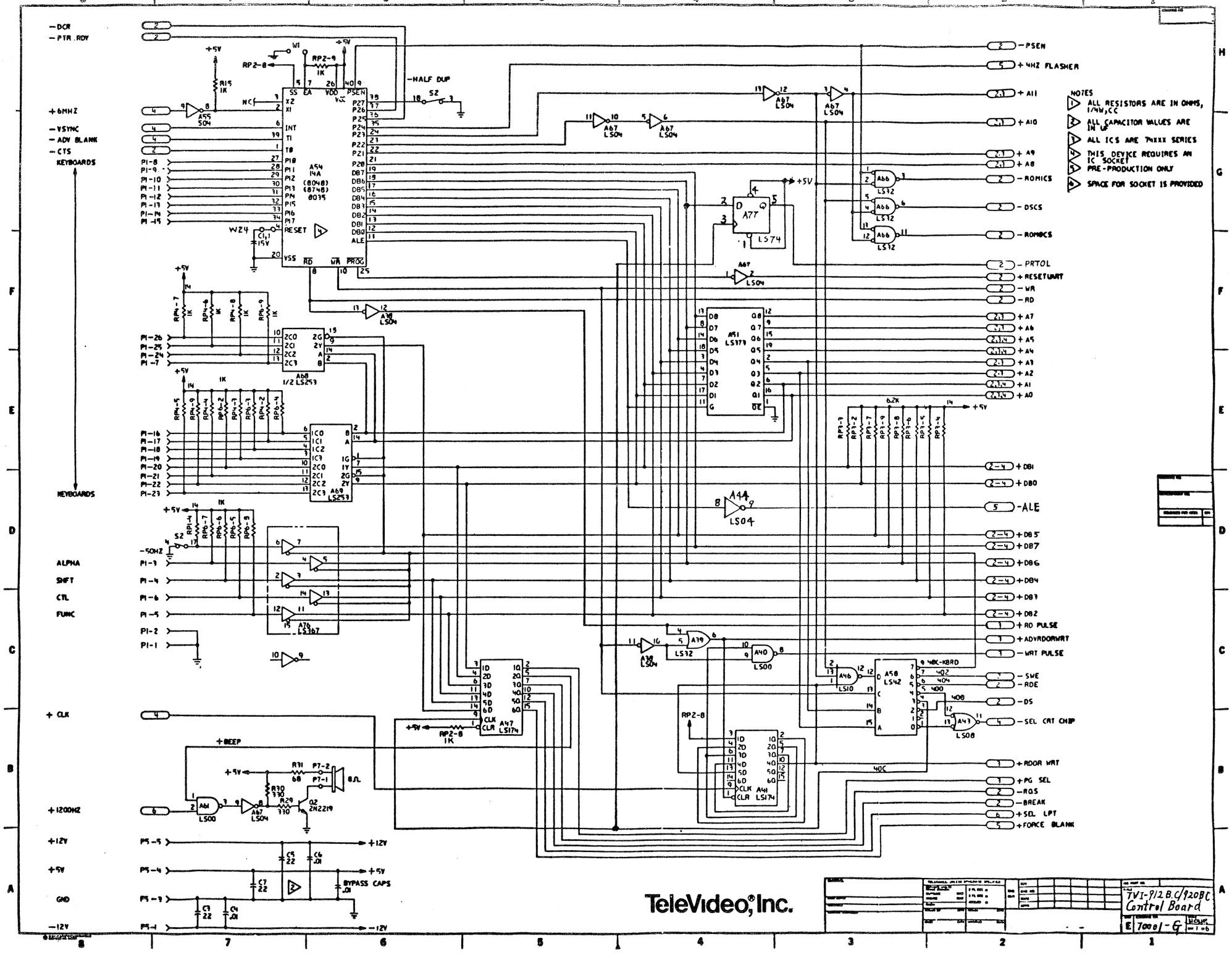
ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	K	L	E	G	H							
84	1	1	0	1	1					RP3	Res Pack 6.2K Ohm	2040700
85		1								R43	Res C/F 10K Ohm 5% 1/4W	2033300
86	2	2	2	2	2					Q1,2	TR 2N4401	2045500
87	3	3	3	3	3					D1,2,3	Diode 1N914	2047500
88		1									P6KE15A Diode	2047900

NOTES:

TITLE CONTROL BOARD, TVI-912/920 TERMINAL

DATE 2-1-83

TeleVideo Systems, Inc.


-DCR
-PTR .RDY
+6MHZ
-VSYNC
-ADV BLANK
-CTS
KEYBOARDS
KEYBOARDS
ALPHA
SHIFT
CTL
FUNC
+CLK
+1200HZ
+12V
+5V
GND
-12V
-50HZ
+BEEP
-HALF DUP
A54 14A (8048) (8748) 8035
A51 LS379
A77 LS74
A67 LS04
A68 1/2 LS253
A69 LS253
A70 LS367
A47 LS174
A44 LS04
A66 LS00
A39 LS32
A40 LS00
A46 LS10
A58 LS42
A43 LS08
A66 LS32
2N2219
-PSEN
+4MZ FLASHER
+A11
+A10
+A9
+A8
-ROMCS
-DSCS
-ROMOCS
-PRTOL
+RESETUART
-WR
-RD
+A7
+A6
+A5
+A4
+A3
+A2
+A1
+A0
+DB1
+DB0
-ALE
+DB5
+DB7
+DB6
+DB4
+DB3
+DB2
+RD PULSE
+ADVRDORWRT
-WRT PULSE
-SWE
-RDE
-DS
-SEL CRT CHIP
+RDOR WRT
+PG SEL
-RQS
-BREAK
+SEL LPT
+FORCE BLANK
NOTES
ALL RESISTORS ARE IN OHMS, 1/4W,CC
ALL CAPACITOR VALUES ARE IN uF
ALL ICS ARE 74xxx SERIES
THIS DEVICE REQUIRES AN IC SOCKET
PRE-PRODUCTION ONLY
SPACE FOR SOCKET IS PROVIDED
BYPASS CAPS .01
TeleVideo, Inc.
TVI-912B,C/920B,C Control Board
E 7008I-G

+A11
-ROMICS
-PSEN
+A10
+A9
+A8
+A7
+A6
+A5
+A4
+A3
+A2
+A1
+A0
-ROMSCS
-PRTDL
-RD
-WR
-DSCS
TELEPHONE INTERFACE P8-1 P8-6 P8-7 P8-8 → P6-11 P6-12 P6-13 P6-14
-SWE
-DS
-RDE
+BAUD GEN
+RESETUART
RCVD(RS232) P3-3 P6-5 P6-6
RXDI(TTY) P3-12
RXD2(TTY) P3-24
+SEL LPT
-BREAK
-RQS
CTS(RS232) P3-5 P6-9 P6-10
DSR(RS232) P3-6
DCD(RS232) P3-8
+PRTRDY(RS232) P4-20
+DB7
+DB6
+DB5
+DB4
+DB3
+DB2
+DB1
+DB0
-SELLPT
-CTS
-DCR
-PRT DY
P3-25 TXDI(TTY)
P3-17 TXD2(TTY)
P3-2 TXD(RS232) P6-4
P4-3 PRT DATA(RS232)
P3-4 RTS(RS232) P6-8
P3-20 DTR(RS232)
P4-8 TERM RDY
P4-6 TERM RDY(RS232)
P3-7 TELEPHONE INTERFACE P4-7
(NOT USED)
A49 2716E 8316E (2716)
A50 2716E 8316E (2716)
A52 8111A OR (2111A)
A53 8111A OR (2111A)
A68 IC3 IC2 IC1 IC0 LS253
A78 LS157
A69 TIL117
A60 75189
A62 LS04
A61 LS00
A59 75188
A48 COM2502/M
R37 1K +5V
S2
S4
RP5-2
RP1-8 RP2-7 RP3-6 RP4-5 RP2-8
R20 3.3K
R19 260
R32 3.3K
R18 3.3K
R17 3.3K
R22 180
R28 100 (OPT)
R29 1M
R25 470
D2 1N914
D3 1N914
W8 W9 W22 W23 W34 W14 W15 W16 W17 W18 W12
S5
+5V +12V -12V
TeleVideo, Inc.
E 7001-G

DISPLAY RAM ADDRESS

+ RAMA9
A9
A10
A2
A5
A4
A1
A7
A6
A8
+ RAMA8

+ A9
A9
A10
A2
A5
A4
A1
A7
A6
A8
+ A0

A24 LS157
A25 LS157
A26 LS157

A27 LS139
-CS3
-CS2
-CS1
-CS0

+ PG SEL

+5V
4.7K
A21 LS86

A13 DP8304
B⇔A
T⇔R
DIR T/R
EN

+ D87
+ D80
+ RD PULSE

+ RD OR WRT
+ A11

A40 LS00
A39 LS32

+ ADV RD OR WRT
- WRT PULSE

2114-3
OPT

+ DISPDATA 7
+ DISPDATA 0
- CPACC

REVISED PER SHEET 6

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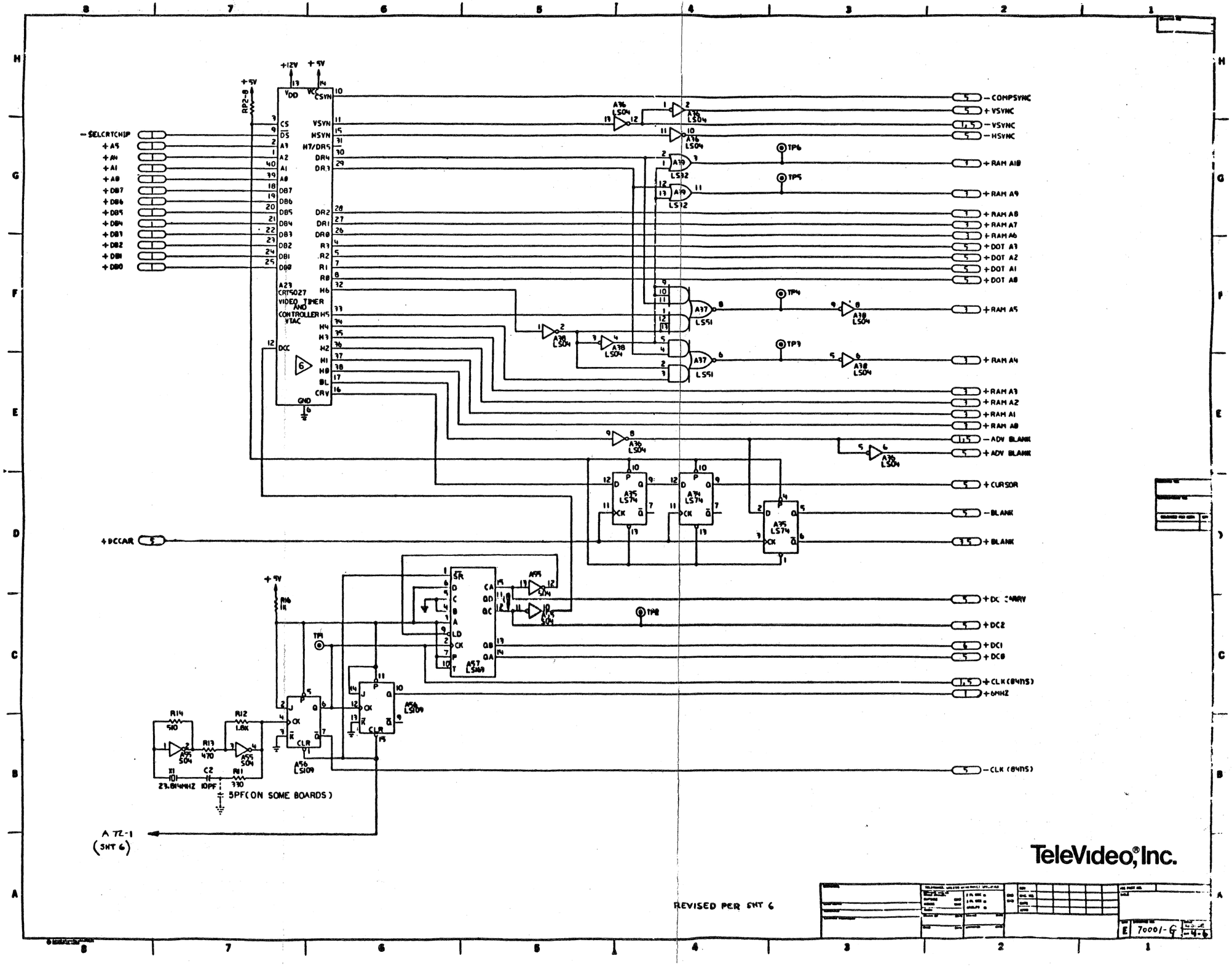
E 7000/-G -3-6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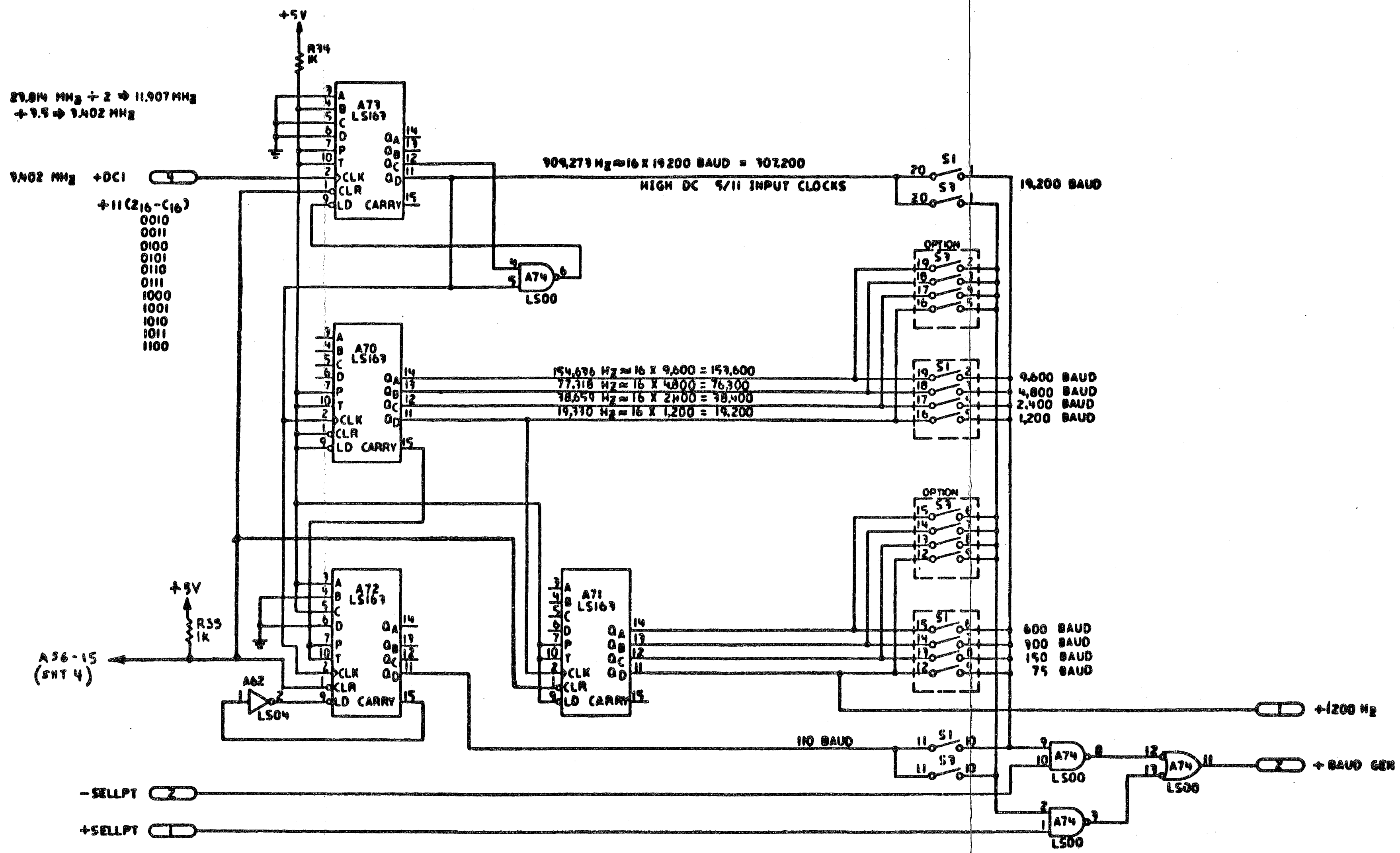
+5V
RP2-8
VDD
VCC
CRT5027
VIDEO TIMING AND CONTROLLER
VTAC
GND
CSYN
VSYN
HSYN
H7/DR5
DR4
DR3
DR2
DR1
DR0
R3
R2
R1
R0
H6
H5
H4
H3
H2
H1
H0
BL
CRV
DCC
CS
DS
A1
A2
A1
A0
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
-SELCRTCHIP
+A5
+A4
+A3
+A2
+A1
+A0
+DB7
+DB6
+DB5
+DB4
+DB3
+DB2
+DB1
+DB0
-COMPSYNC
+VSYNC
-VSYNC
-HSYNC
+RAM A10
+RAM A9
+RAM A8
+RAM A7
+RAM A6
+DOT A3
+DOT A2
+DOT A1
+DOT A0
+RAM A5
+RAM A4
+RAM A3
+RAM A2
+RAM A1
+RAM A0
-ADV BLANK
+ADV BLANK
+CURSOR
-BLANK
+BLANK
+DCCARR
+DC CARRY
+DC2
+DC1
+DC0
+CLK (84MHZ)
+6MHZ
-CLK (84MHZ)
TP6
TP5
TP4
TP3
TP2
TP1
A39 LS32
A37 LS51
A35 LS74
A34 LS74
A35 LS74
A57 LS169
A56 LS109
A55 LS04
A36 LS04
A38 LS04
R14 510
R12 1.8K
R13 470
R1 330
C2 10PF
X1 23.814MHZ
5PF(ON SOME BOARDS)
A 72-1 (SHT 6)
REVISED PER SHT 6
TeleVideo, Inc.
E
7000/-6

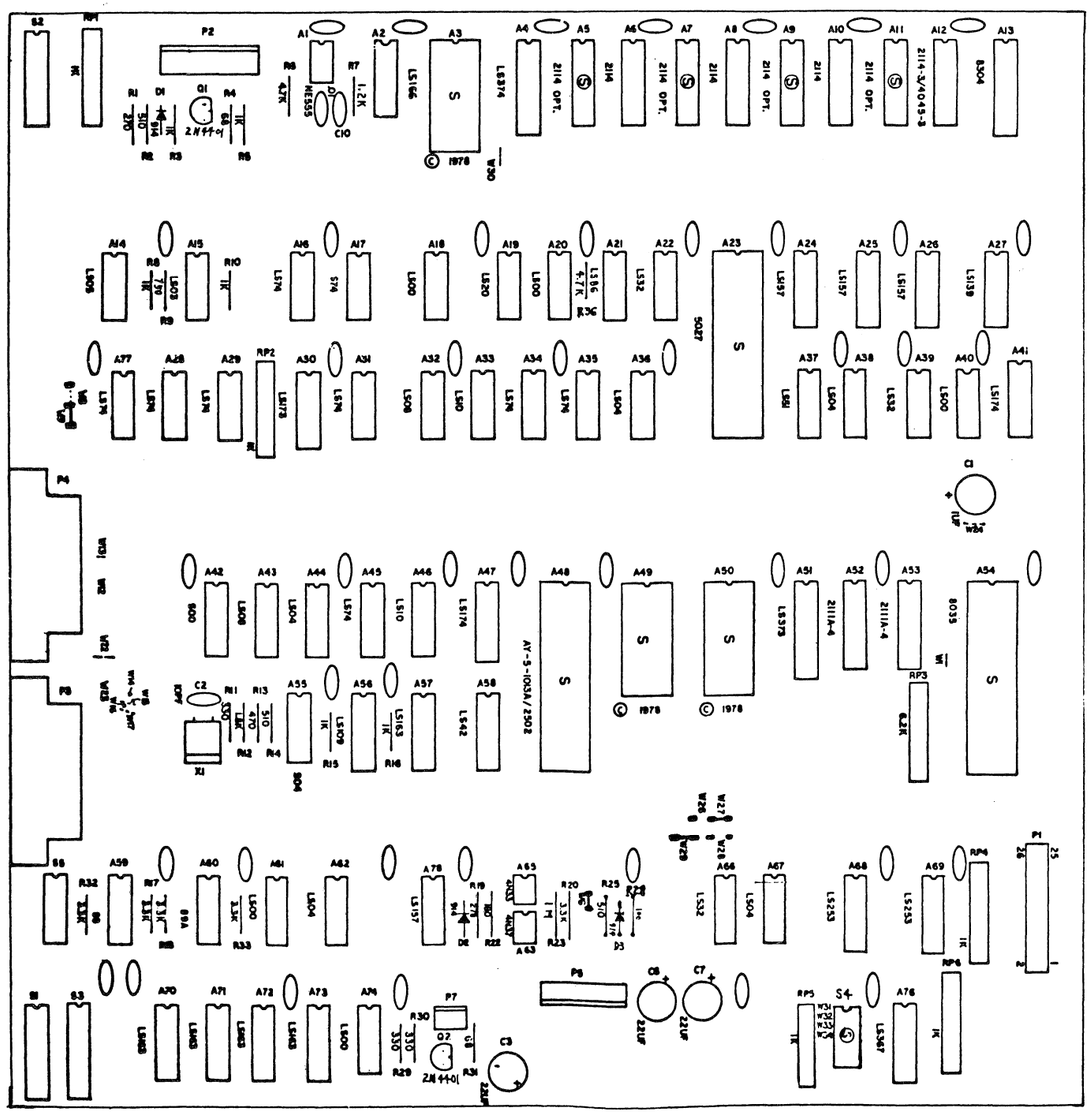
+CURSOR
+4HZ FLASHER
-BLANK
+ADV BLANK
-VSYNC
-10TH DOT ROW
1ST LINE
+DOTA3
+DOTA2
+DOTA1
+DOTA0
+5V
+DC0
-ALE
-CPACC
+DC2
+DISP DATA 7
+DISP DATA 0
+DC CARRY
+CLK
-CLK
-ADV BLANK
-CONTROL
+V SYNC
+BLANK
+FORCE BLANK
-COMP SYNC
-H SYNC
CURS FLASH
PROTECT =1/2 INTENSITY
+DCCAR
"2716" W30
LOW
+DRD0
+DRD1
+DRD2
+DRD3
+DRD4
+DRD5
+DRD6
+DRD7
2716E
UNDERLINE
INVERT VIDEO
+VIDEO
VIDEO SHIELD GND (+TTL VIDEO)
+V SYNC
+HSYNC
A62 LS04
A14 LS05 (O.C.)
A44 LS04
A55 S04
TeleVideo, Inc.



BAUD RATE GENERATION

TeleVideo®, Inc.

E 70001-G



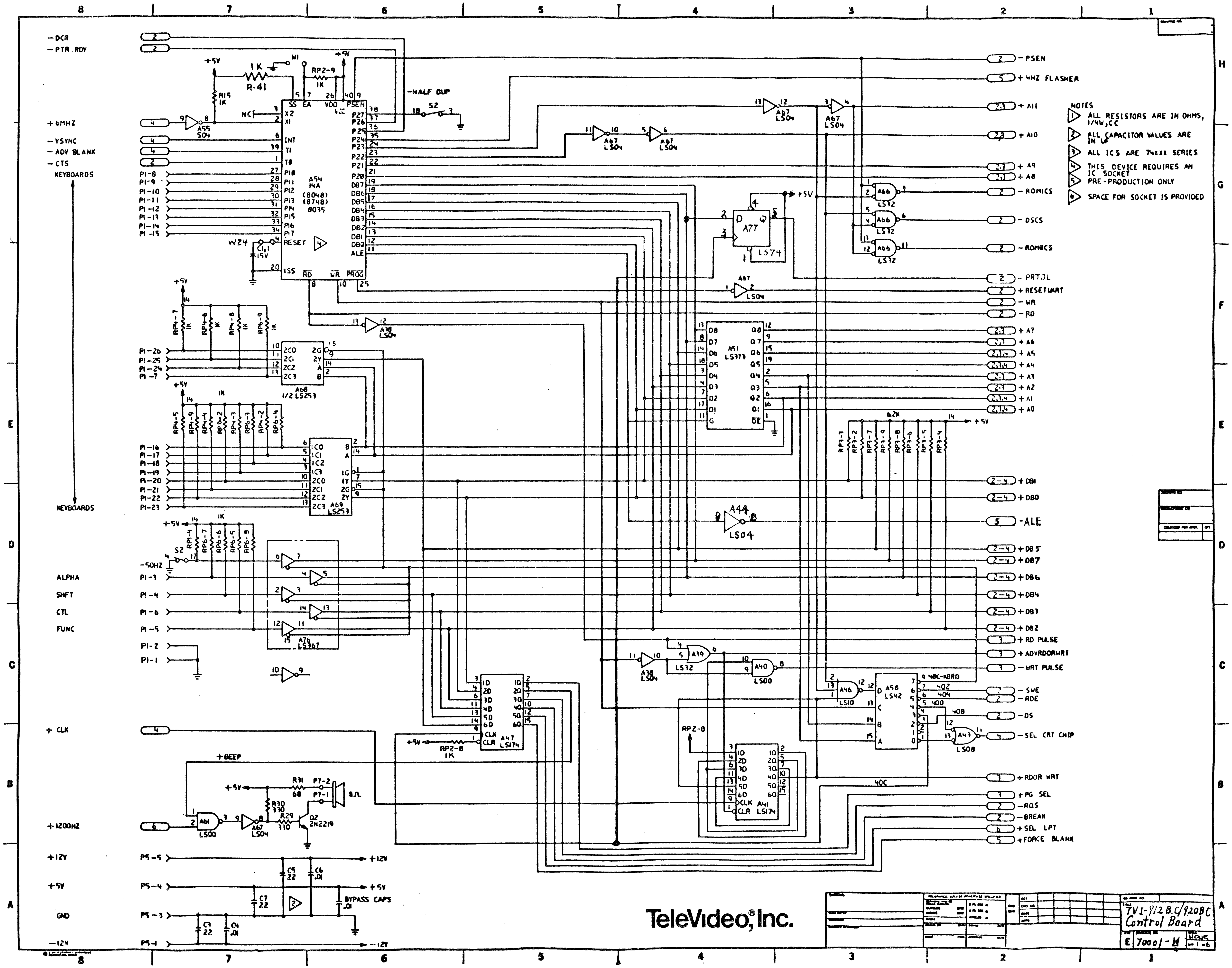
Note

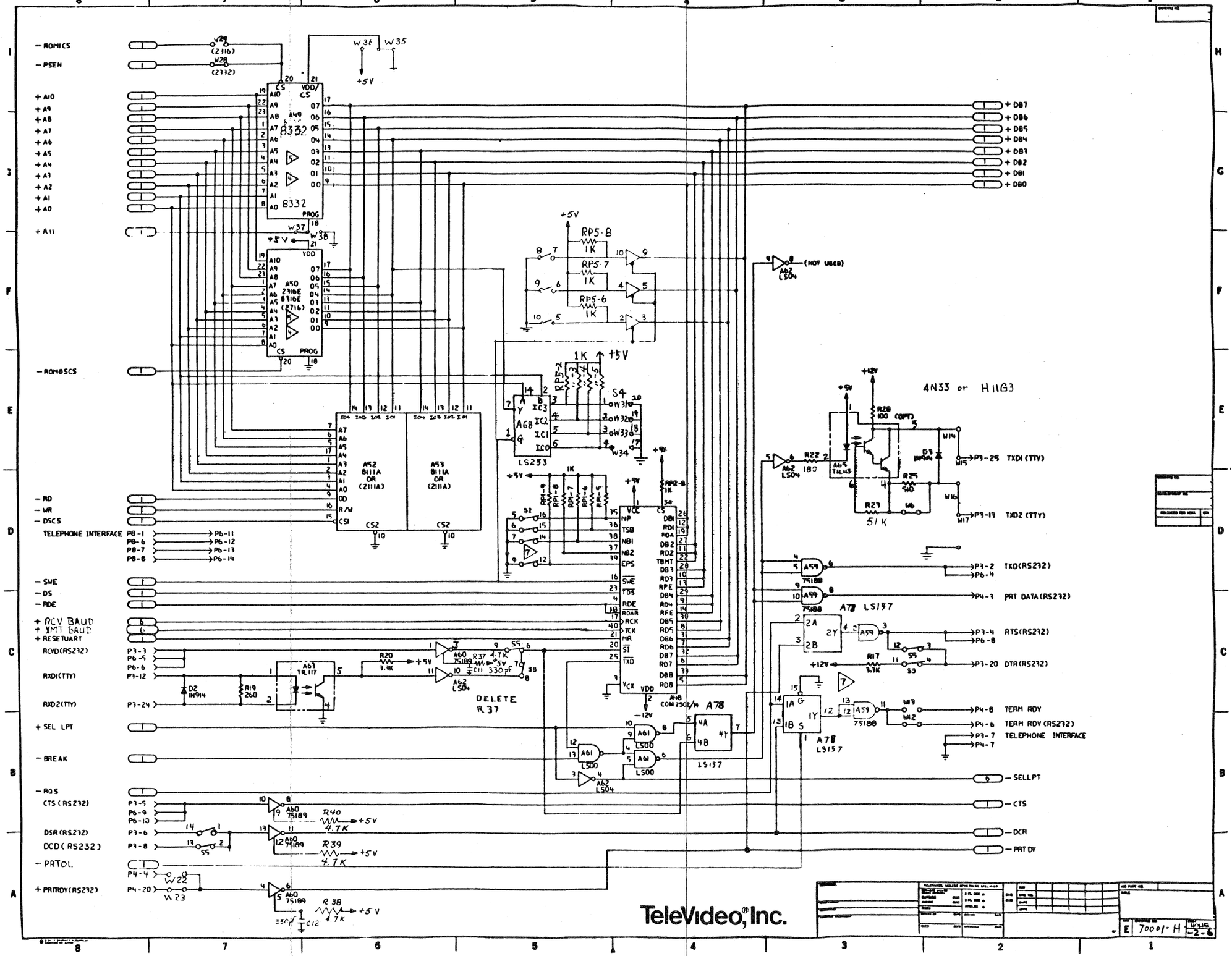
1. ⓢ shows sockets only are mounted at those locations. A5. A7. A9, A11 and S4.
2. S shows chips are mounted on socket at A3. A23. A49. A50 and A54.
3. For 2nd page memory option, add 2114 chips at A5. A7. A9 and A11.

12-72

TeleVideo, Inc.
3190 Coronado Dr. Santa Clara, CA 95051

TOLERANCES (UNLESS OTHERWISE NOTED)	REVISIONS			ASSEMBLY DRAWING		
DECIMAL ±	NO	DATE	BY	TVI-912 B.C/920 B.C CONTROL BOARD		
FRACTIONAL ±	1			DRAWN BY	SCALE	MATERIAL
ANGULAR ±	2			CHK'D	DATE	DRAWING NO
	3			TRACED	APP'D	70001-G
	4					
	5					


NOTES
1. ALL RESISTORS ARE IN OHMS, 1/4W, CC
2. ALL CAPACITOR VALUES ARE IN uF
3. ALL ICS ARE 74xxx SERIES
4. THIS DEVICE REQUIRES AN IC SOCKET
5. PRE-PRODUCTION ONLY
6. SPACE FOR SOCKET IS PROVIDED
-DCR
-PTR RDY
+6MHZ
-VSYNC
-ADV BLANK
-CTS
KEYBOARDS
ALPHA
SHFT
CTL
FUNC
+CLK
+BEEP
+1200HZ
+12V
+5V
GND
-12V
BYPASS CAPS
-HALF DUP
A54 14A (8048) (8748) 8035
-PSEN
+4HZ FLASHER
+A11
+A10
+A9
+A8
-ROMICS
-DSCS
-ROM0CS
-PRTOL
+RESETUART
-WR
-RD
+A7
+A6
+A5
+A4
+A3
+A2
+A1
+A0
+DB1
+DB0
-ALE
+DB5
+DB7
+DB6
+DB4
+DB3
+DB2
+RD PULSE
+ADVRDORWRT
-WRT PULSE
-SWE
-RDE
-DS
-SEL CRT CHIP
+RDOR WRT
+PG SEL
-RQS
-BREAK
+SEL LPT
+FORCE BLANK
TeleVideo, Inc.
TVI-912 B.C/920BC Control Board
E 70001-H


-ROMICS
-PSEN
+A10
+A9
+A8
+A7
+A6
+A5
+A4
+A3
+A2
+A1
+A0
+A11
-ROMOSCS
-RD
-WR
-DSCS
TELEPHONE INTERFACE P8-1 → P6-11
P8-6 → P6-12
P8-7 → P6-13
P8-8 → P6-14
-SWE
-DS
-RDE
+RCV BAUD
+XMT BAUD
+RESETUART
RCVD(RS232) P3-3 P6-5 P6-6
RXDI(TTY) P3-12
RXD2(TTY) P3-24
+SEL LPT
-BREAK
-RQS
CTS(RS232) P3-5 P6-9 P6-10
DSR(RS232) P3-6
DCD(RS232) P3-8
-PRTDL
P4-4
+PRTRDY(RS232) P4-20
W22
W23
W28 (2732)
W29 (2716)
W36
W35
+5V
W37
W38
A49 8332
A50 2716E 8316E (2716)
A52 8111A OR (2111A)
A53 8111A OR (2111A)
+DB7
+DB6
+DB5
+DB4
+DB3
+DB2
+DB1
+DB0
RP5-8 1K
RP5-7 1K
RP5-6 1K
RP5-2 1K
RP4-9 1K
RP4-8 1K
RP4-7 1K
RP4-6 1K
RP4-5 1K
RP2-8 1K
A68 LS253
A78 CDN2502/N
A78 LS157
A60 75189
A62 LS04
A63 TIL117
A61 LS00
A59 75188
A69 TIL113
D2 IN914
D3 IN4744
R19 260
R20 3.9K
R37 4.7K
C11 330pF
C12 330pF
R40 4.7K
R39 4.7K
R38 4.7K
R22 180
R23 51K
R25 510
R28 100 (OPT)
R17 3.3K
DELETE R37
4N33 or H11G3
(NOT USED)
P3-25 TXDI (TTY)
P3-13 TXD2 (TTY)
P3-2 TXD(RS232)
P6-4
P4-3 PRT DATA(RS232)
P3-4 RTS(RS232)
P6-8
P3-20 DTR(RS232)
P4-8 TERM RDY
P4-6 TERM RDY(RS232)
P3-7 TELEPHONE INTERFACE
P4-7
-SELLPT
-CTS
-DCR
-PRTDY
TeleVideo, Inc.
E 70001-H

DISPLAY RAM ADDRESS

+ RAMA13
A9
A10
A2
A5
A4
A1
A7
A6
A8
+ RAMA8

+ A13
A9
A10
A2
A5
A4
A1
A7
A6
A8
+ A0

A24 LS157
A25 LS157
A26 LS157

+ PG SEL
A27 LS139
-CS3
-CS2
-CS1
-CS0

+5V
R36 4.7K
A21 LS86

+ DB7
6
5
4
3
2
1
+ DB0
+ RD PULSE
A13 DP8304 B⇔A T⇔R DIR T/R EN

+ RD OR WRT
+ A11
A40 LS00
A40 LS00
A40 LS00
A39 LS32
+ ADV RD OR WRT
- WRT PULSE

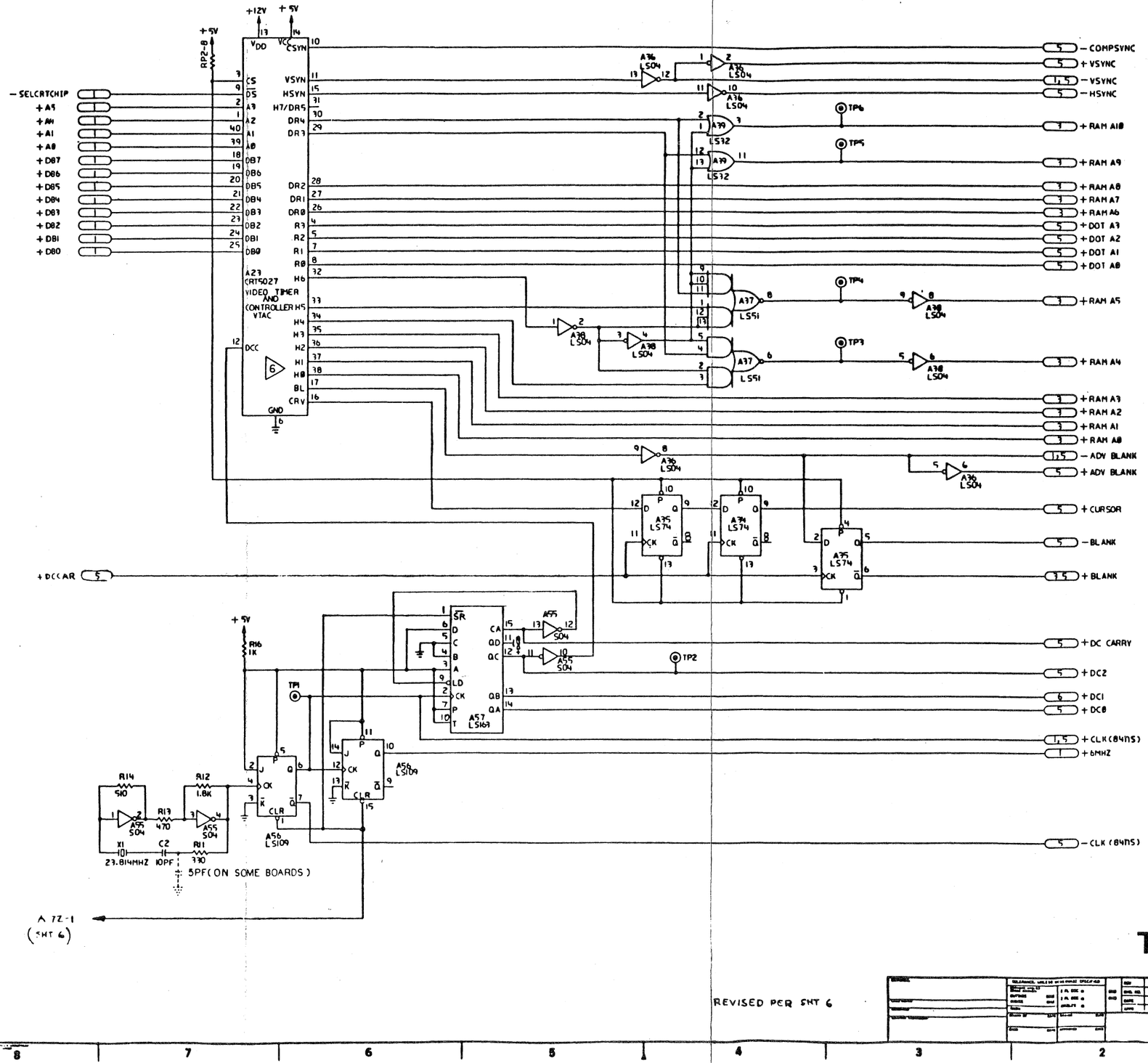
2114-3 OPT

+ DISPDATA 7
6
5
4
3
2
1
+ DISPDATA 0
- CPACC

REVISED PER SHEET 6

TeleVideo, Inc.

E 70001-H

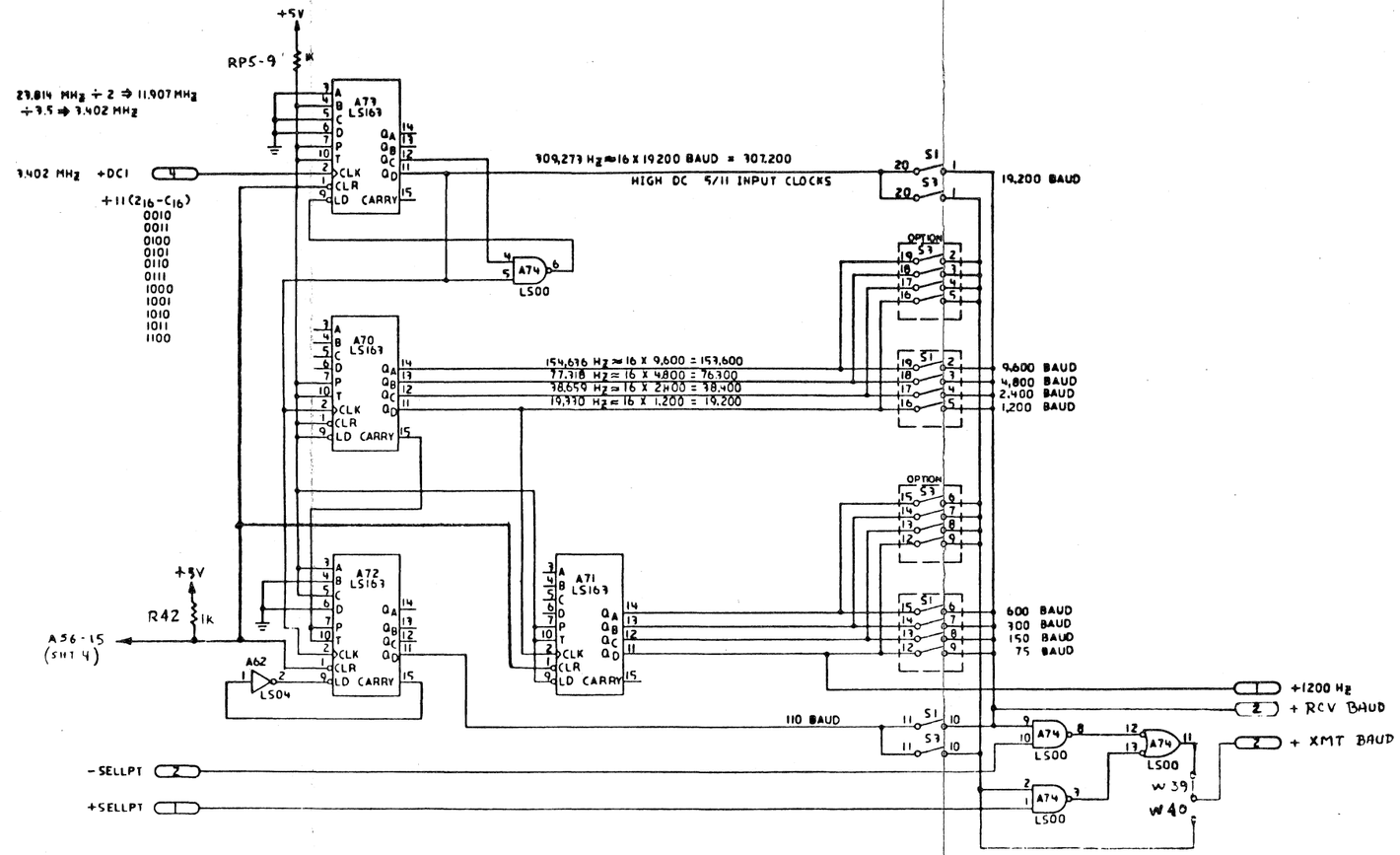

+12V
+5V
RP2-8
- SELCRTCHIP
+A5
+A4
+A3
+A2
+A1
+A0
+DB7
+DB6
+DB5
+DB4
+DB3
+DB2
+DB1
+DB0
CRT5027
VIDEO TIMER AND CONTROLLER VTAC
- COMPSYNC
+ VSYNC
- VSYNC
- HSYNC
+ RAM A10
+ RAM A9
+ RAM A8
+ RAM A7
+ RAM A6
+ DOT A3
+ DOT A2
+ DOT A1
+ DOT A0
+ RAM A5
+ RAM A4
+ RAM A3
+ RAM A2
+ RAM A1
+ RAM A0
- ADV BLANK
+ ADV BLANK
+ CURSOR
- BLANK
+ BLANK
+ DCCAR
+ DC CARRY
+ DC2
+ DC1
+ DC0
+ CLK (64NS)
+ 6MHZ
- CLK (64NS)
TP6
TP5
TP4
TP3
TP2
TP1
A39 LS32
A37 LS51
A38 LS04
A36 LS04
A35 LS74
A34 LS74
A57 LS163
A56 LS109
A55 S04
R16 1K
R14 510
R12 1.8K
R13 470
R11 330
X1 23.814MHZ
C2 10PF
5PF (ON SOME BOARDS)
A 72-1 (SHT 6)
REVISED PER SHT 6
TeleVideo, Inc.
E 70001-H

+CURSOR
+4HZ FLASHER
-BLANK
+ADV BLANK
-VSYNC
-10TH DOT ROW
1ST LINE
+DOTA3
+DOTA2
+DOTA1
+DOTA0
+DC0
-ALE
-CPACC
+DC2
+DISP DATA 7
+DISP DATA 0
+DC CARRY
+CLK
-CLK
-ADV BLANK
-CONTROL
+V SYNC
+BLANK
+FORCE BLANK
-COMP SYNC
-H SYNC
CURS FLASH
PROTECT =1/2 INTENSITY
+DCCAR
UNDERLINE
INVERT VIDEO
+VIDEO
VIDEO SHIELD GND (+TTL VIDEO)
+V SYNC
+HSYNC

A62 LS04
A36 LS04
A14 LS05 (O.C.)
A62 LS04
A55 S04
A20 LS00

TeleVideo, Inc.

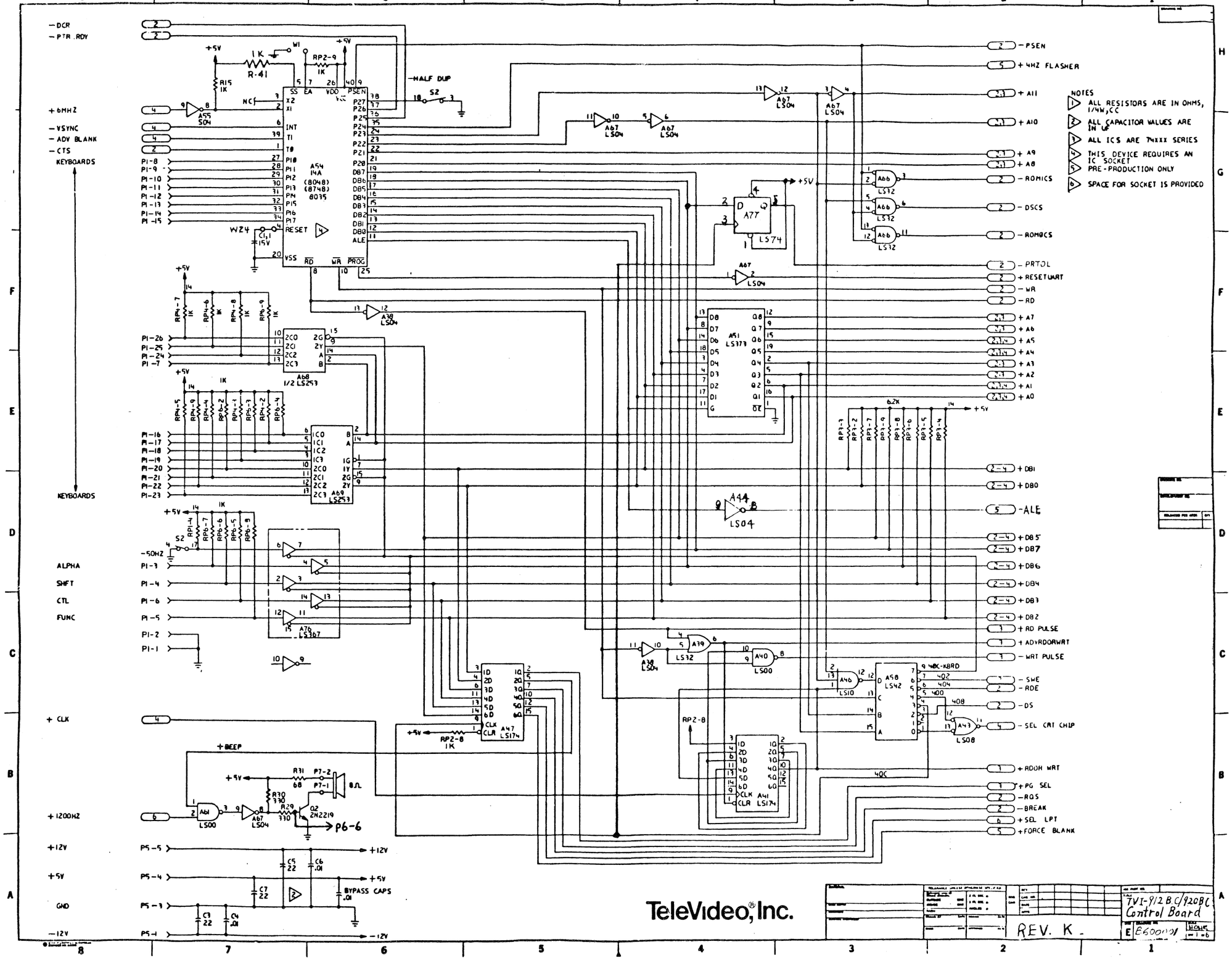
E 7000/-H -5-6

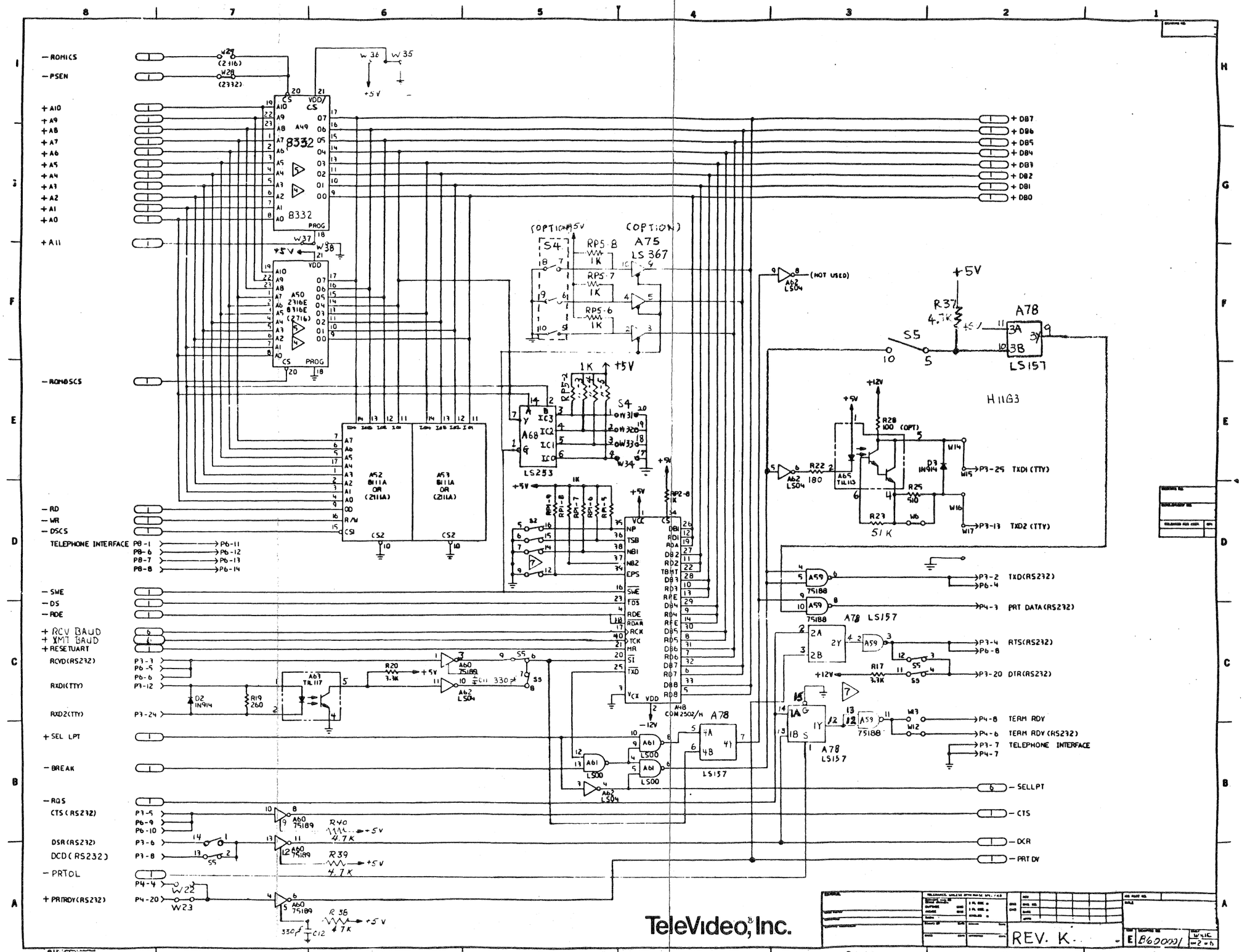


BAUD RATE GENERATION

TeleVideo, Inc.

E 70001-H


NOTES
ALL RESISTORS ARE IN OHMS, 1/4W, CC
ALL CAPACITOR VALUES ARE IN UF
ALL ICS ARE 74XXX SERIES
THIS DEVICE REQUIRES AN IC SOCKET
PRE-PRODUCTION ONLY
SPACE FOR SOCKET IS PROVIDED
-DCR
-PTR. RDY
+6MHZ
-VSYNC
-ADV BLANK
-CTS
KEYBOARDS
ALPHA
SHFT
CTL
FUNC
+ CLK
+1200HZ
+12V
+5V
GND
-12V
-50HZ
+BEEP
-HALF DUP
+PSEN
+4HZ FLASHER
+A11
+A10
+A9
+A8
-ROM1CS
-DSCS
-ROM0CS
-PRTOL
+RESETUART
-WR
-RD
+A7
+A6
+A5
+A4
+A3
+A2
+A1
+A0
+DB1
+DB0
-ALE
+DB5
+DB7
+DB6
+DB4
+DB3
+DB2
+RD PULSE
+ADVRDORWRT
-WRT PULSE
-SWE
-RDE
-DS
-SEL CAT CHIP
+RDOH WRT
+PG SEL
-RQS
-BREAK
+SEL LPT
+FORCE BLANK
TeleVideo, Inc.
TVI-912B C/920B C Control Board
REV. K
E 8600101


-ROMICS
-PSEN
+A10
+A9
+A8
+A7
+A6
+A5
+A4
+A3
+A2
+A1
+A0
+A11
-ROM0SCS
-RD
-WR
-DSCS
TELEPHONE INTERFACE P8-1 → P6-11
P8-6 → P6-12
P8-7 → P6-13
P8-8 → P6-14
-SWE
-DS
-RDE
+RCV BAUD
+XMT BAUD
+RESET UART
RCVD(RS232) P3-3, P6-5
RXDI(TTY) P6-6, P3-12
RXD2(TTY) P3-24
+SEL LPT
-BREAK
-RQS
CTS(RS232) P3-5, P6-9, P6-10
DSR(RS232) P3-6
DCD(RS232) P3-8
-PRTDL P4-4
+PRTRDY(RS232) P4-20
8332
2716
A52 8111A OR (2111A)
A53 8111A OR (2111A)
A49
A50 2316E 8316E (2716)
A48 COM2502/H
A78
A75 LS367
A68 LS253
A63 TIL117
A60 75189
A61 LS00
A62 LS504
A59 75188
A65 TIL113
LS157
H11G3
(OPTION) +5V
(OPTION) A75 LS367
RPS-8 1K
RPS-7 1K
RPS-6 1K
S4
S5
W20 (2716)
W28 (2732)
W36
W35
W37
W38
+5V
+12V
-12V
1K
R37 4.7K
R28 100 (OPT)
R22 180
R25 510
R23 51K
D3 IN914
D2 IN914
R19 260
R20 3.3K
R40 4.7K
R39 4.7K
R36 4.7K
C11 330pf
C12 330pf
W22
W23
(NOT USED)
P3-25 TXDI (TTY)
P3-13 TXD2 (TTY)
P3-2 TXD(RS232)
P6-4
P4-3 PRT DATA(RS232)
P3-4 RTS(RS232)
P6-8
P3-20 DTR(RS232)
P4-8 TERM RDY
P4-6 TERM RDY(RS232)
P3-7 TELEPHONE INTERFACE
P4-7
-SELLPT
-CTS
-DCR
-PRT DV
+DB7
+DB6
+DB5
+DB4
+DB3
+DB2
+DB1
+DB0
TeleVideo, Inc.
REV. K
B600001

DISPLAY RAM ADDRESS

+ RAMA3
A9
A10
A2
A5
A4
A1
A7
A6
A8
+ RAMA8

+ A3
A9
A10
A2
A5
A4
A1
A7
A6
A8
+ A0

A24 LS157
A25 LS157
A26 LS157

A27 LS139
+ PG SEL
-CS3
-CS2
-CS1
-CS0

+5V
R36 4.7K
A21 LS86

A13 DP8304
+ DB7
+ DB0
+ RD PULSE
B⇔A
T⇔R
DIR T/R
EN

+ RD OR WRT
+ A11
A40 LS00
A39 LS32
+ ADV RD OR WRT
- WRT PULSE

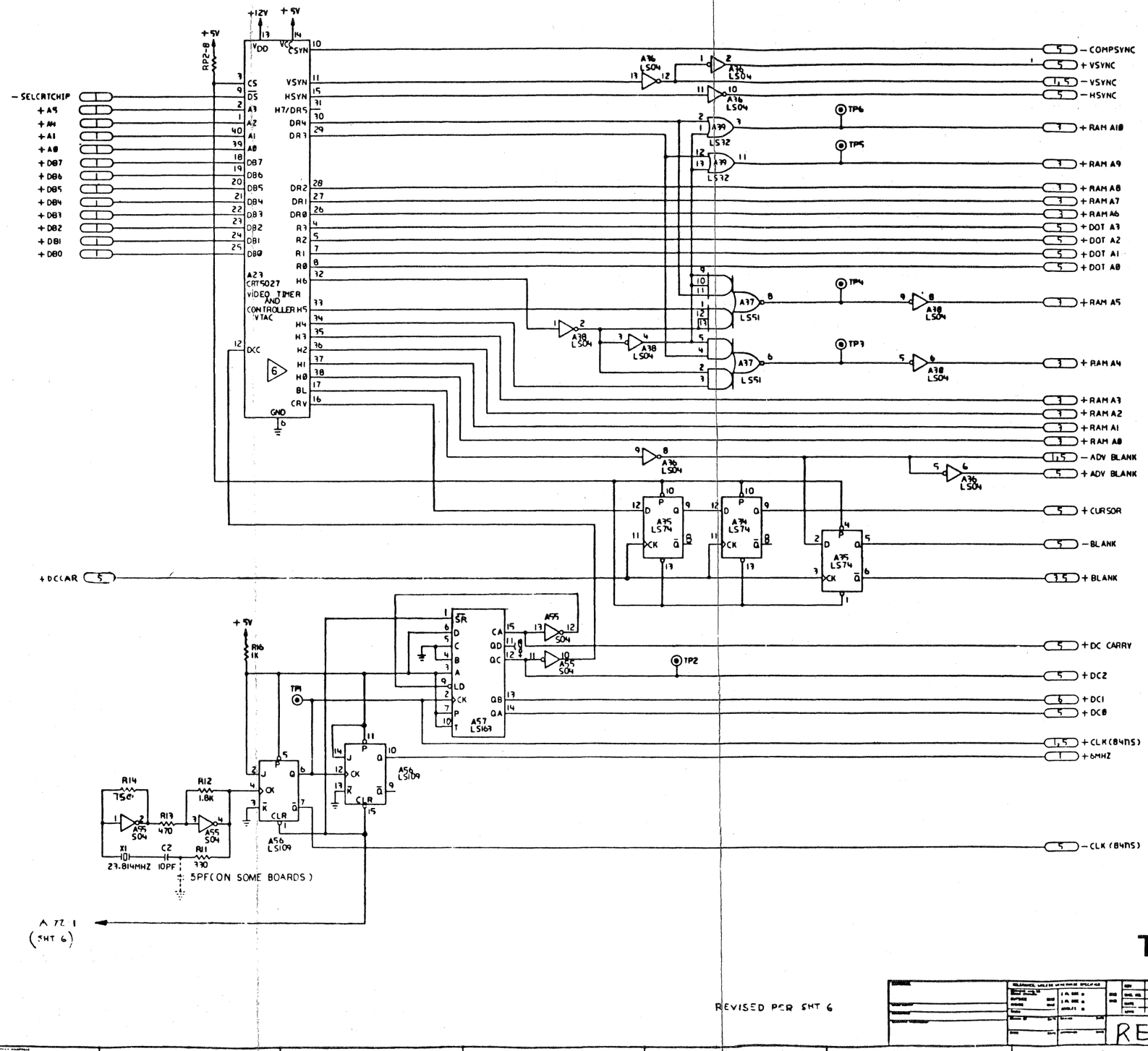
2114-3
WE
CS
OPT

+ DISPDATA 7
+ DISPDATA 0
- C PACC

TeleVideo, Inc.

REVISED PER SHEET 6

REV. K

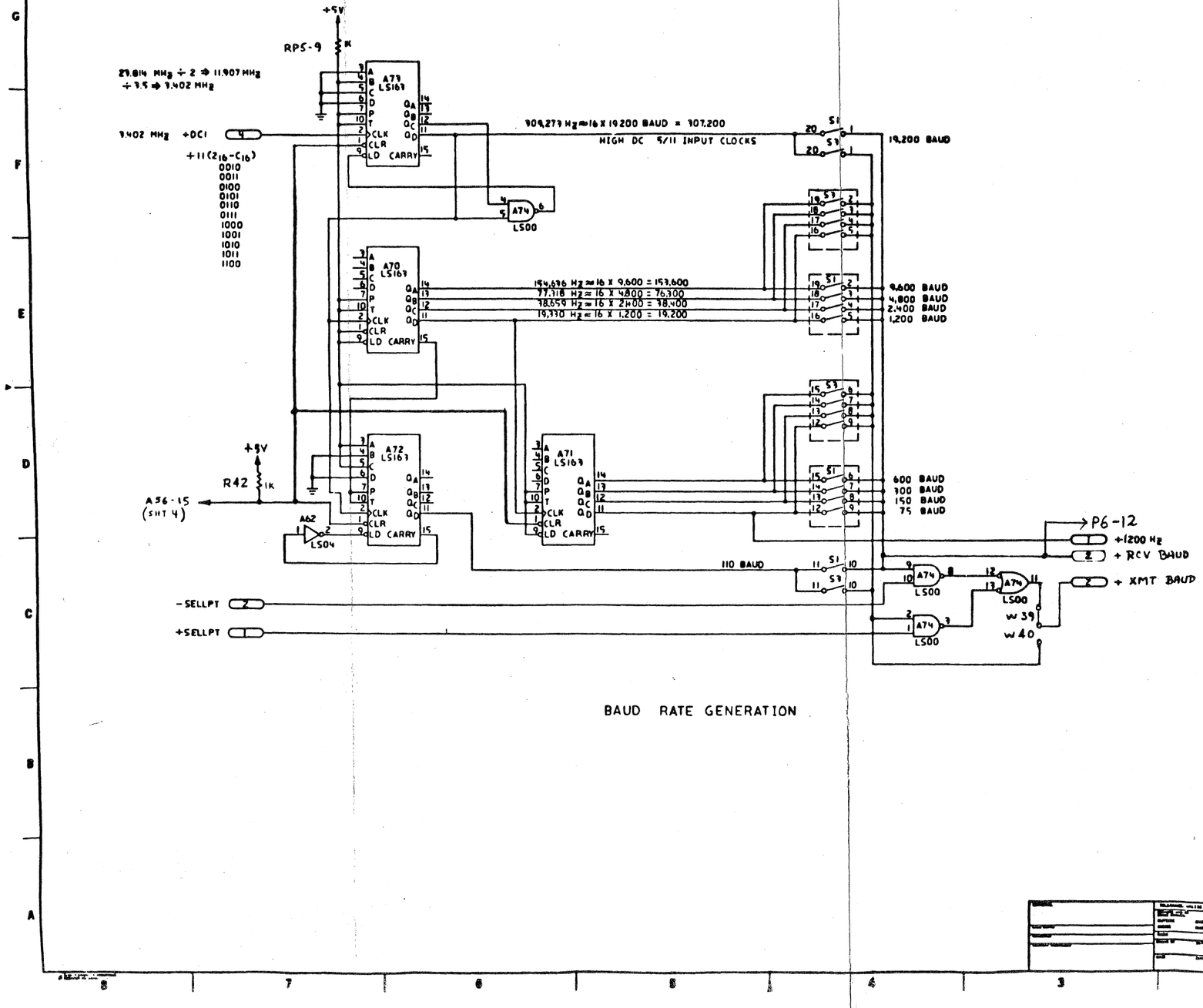

+12V
+5V
RP2-8
VDD
VCC
CSYN
VSYN
HSYN
H7/DR5
DR4
DR3
DR2
DR1
DR0
R3
R2
R1
R0
H6
H5
H4
H3
H2
H1
H0
BL
CRV
GND
DCC
CS
DS
A23
CRT5027
VIDEO TIMER AND CONTROLLER VTAC
- SELCRTCHIP
+ A9
+ A4
+ A1
+ A0
+ DB7
+ DB6
+ DB5
+ DB4
+ DB3
+ DB2
+ DB1
+ DB0
A36 LS04
A39 LS32
A37 LS51
A38 LS04
TP6
TP5
TP4
TP3
TP2
TP1
- COMPSYNC
+ VSYNC
- VSYNC
- HSYNC
+ RAM A10
+ RAM A9
+ RAM A8
+ RAM A7
+ RAM A6
+ DOT A3
+ DOT A2
+ DOT A1
+ DOT A0
+ RAM A5
+ RAM A4
+ RAM A3
+ RAM A2
+ RAM A1
+ RAM A0
- ADV BLANK
+ ADV BLANK
+ CURSOR
- BLANK
+ BLANK
+ DC CARRY
+ DC2
+ DC1
+ DC0
+ CLK (84NS)
+ 6MHZ
- CLK (84NS)
+ DCCAR
A35 LS74
A34 LS74
A55 S04
A57 LS163
A56 LS109
R16 1K
R14 75Ω
R12 1.8K
R13 470
R11 330
C2 10PF
X1 27.814MHZ
5PF (ON SOME BOARDS)
A 72-1 (SHT 6)
REVISED PER SHT 6
TeleVideo, Inc.
REV. K
B600001-4-6

+CURSOR
+4HZ FLASHER
-BLANK
+ADV BLANK
-VSYNC
-10TH DOT ROW
1ST LINE
+DOTA3
+DOTA2
+DOTA1
+DOTA0
+DC0
+5V
-ALE
-CPACC
+DC2
+DISP DATA 7 6 5 4 3 2 1
+DISP DATA 0
+DC CARRY
+CLK
-CLK
-ADV BLANK
-CONTROL
+V SYNC
+BLANK
+FORCE BLANK
-COMP SYNC
-H SYNC
CURS FLASH
PROTECT =1/2 INTENSITY
+DCCA7
UNDERLINE
INVERT VIDEO
+VIDEO
VIDEO SHIELD GND (+TTL VIDEO)
+V SYNC
+HSYNC
A62 LS04
A36 LS04
A14 LS05 (O.C.)
A62 LS04
A55 S04
LS00

TeleVideo, Inc.

REV. K

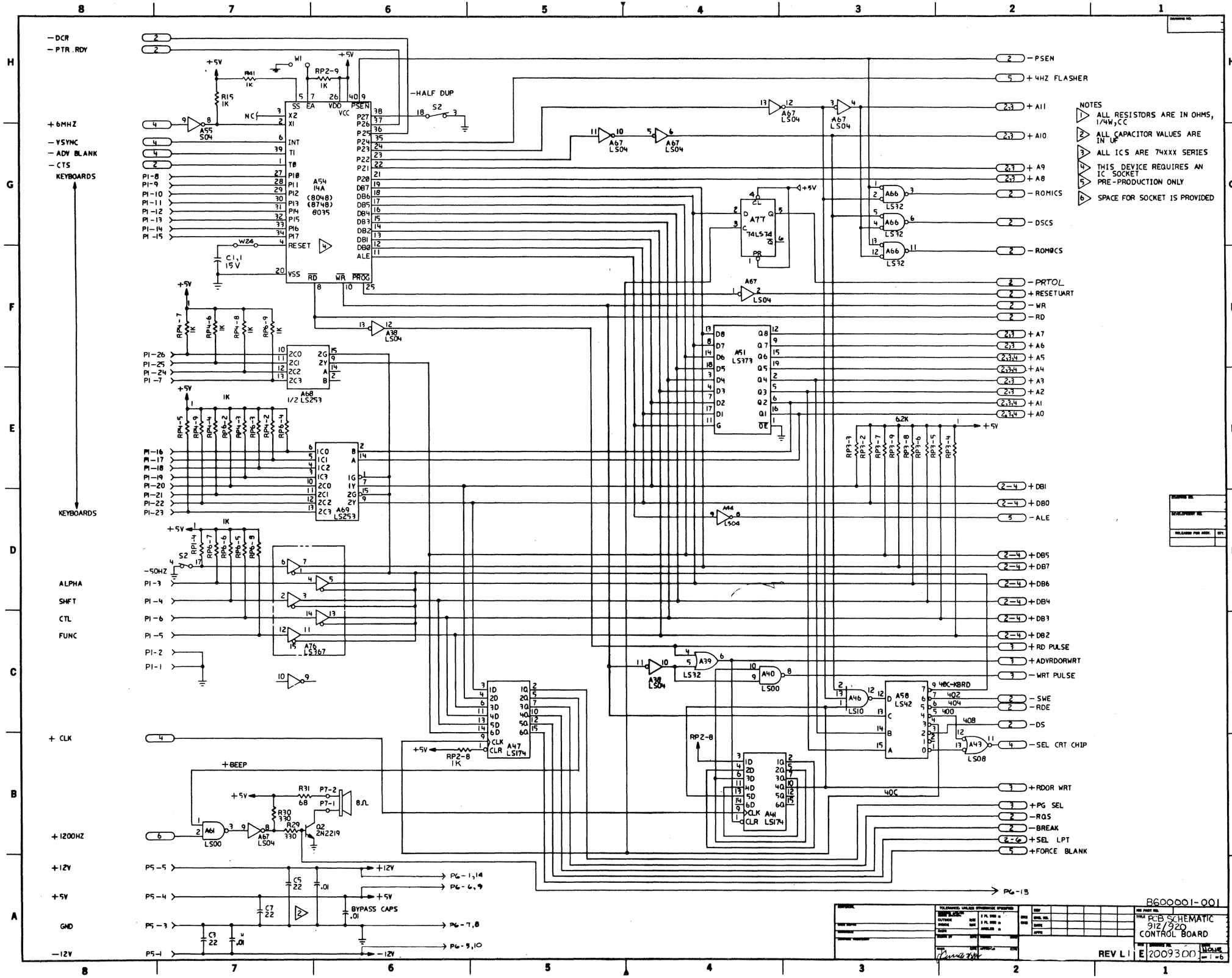
E 8600001 1-5-6



BAUD RATE GENERATION

TeleVideo, Inc.

REV. K


NOTES
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6 SPACE FOR SOCKET IS PROVIDED
-DCR
-PTR.RDY
+6MHZ
-VSYNC
-ADV BLANK
-CTS
KEYBOARDS
KEYBOARDS
-HALF DUP
A54 I4A (8048) (8748) 8035
A55 S04
A67 LS04
A77 74LS74
A51 LS373
A68 1/2 LS253
A69 LS253
A76 LS367
A47 LS174
A38 LS04
A39 LS32
A40 LS00
A44 LS04
A46 LS10
A58 LS42
A66 LS32
A43 LS08
A61 LS00
A67 LS04
A44 LS174
-PSEN
+4HZ FLASHER
+A11
+A10
+A9
+A8
-ROMICS
-DSCS
-ROM0CS
-PRTOL
+RESETUART
-WR
-RD
+A7
+A6
+A5
+A4
+A3
+A2
+A1
+A0
+DB1
+DB0
-ALE
+DB5
+DB7
+DB6
+DB4
+DB3
+DB2
+RD PULSE
+ADVRDORWRT
-WRT PULSE
-SWE
-RDE
-DS
-SEL CRT CHIP
+RDOR WRT
+PG SEL
-RQS
-BREAK
+SEL LPT
+FORCE BLANK
+CLK
+1200HZ
+12V
+5V
GND
-12V
+BEEP
ALPHA
SHFT
CTL
FUNC
-50HZ
P6-13
B600001-001
PCB SCHEMATIC 912/920 CONTROL BOARD
REV L1
E
2009300

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

P7-2
P7-1
P3-5 CTS (RS232)
P7-4
P7-3
-PRTOL
+SEL LPT
-BREAK
-RQS (RS232)
P3-8 DCD (RS232)
P3-6 DSR
P4-Z PRT RCV
P6-3
P3-3 RCVD (RS232)
P3-12 RXD1 (TTY)
P3-24 RXD2 (TTY)
P4-4
P4-20 PRT RDY (RS232)
P7-8
P7-5 +RCV BAUD
P7-10
P7-9 +XMT BAUD
P7-11 RESET UART
-RDE
-DS
P7-6 EDC
-RD
-WR
-DSCS
-ROM0CS
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
-ROM1CS
-PSEN
A11
-SWE

A60 75189
R40 4.7K +5V
A62 74LS04
A66 74LS32
A61 74LS00
A61 74LS00
A61 74LS00
W50
W54
W56
W55
W58
W57
W46
W45
W47
W49
R39 4.7K +5V
R43 10K
R20 3.3K
A60 75189
C11 330pF
A32 74LS08
A62 74LS04
W48
A63 TIL 117
D2 IN914
R19 680
A60 75189
R38 4.7K +5V
W53
C12 330 pF
W22
W23
W43
W44
W29
W28
W36
W35
W38
W37
A60 75189
2332 A49
2316E A50 (2716)
8111A (2111A) A52
8111A (2111A) A53
RP5 1K
S4
A68 LS253
A75 74LS367
(OPTION)

A62 74LS04
R22 180
A69 TIL 113
R26 100 (OPT) +12V
D3 IN914
R25 510
R23 1K
W14
W15
W16
W17
W6
TXD1 (TTY) P3-25
TXD2 (TTY) P3-13
TXD (RS232) P3-2 P6-2
W51
W52
75188 A59
W55
R37 4.7K +5V
A78 74LS157
75188 A59
PRT DATA (RS232) P4-3
W13 TERM RDY (RS232)
W12 TERM RDY (RS232) P4-8 P4-6
RTS (RS232) P3-4
DTR (RS232) P3-20
+12V R17 3.3K
-PRT RDY
-DCR
RP1 1K
S2
RP2-8
A48 COM2502/H
-12V
SIGNAL GND P3-7 P4-7
+DB0
+DB1
+DB2
+DB3
+DB4
+DB5
+DB6
+DB7

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN Sonny 5-14-81
NEXT ASSY	USED ON	ANG ± 2 PLC ± 3 PLC ±	CHK Alexander 7/3/81
		SCALE:	ENGR
		MATERIAL	APPD
			APPD
			APPD
			FINISH

B600001-001

TeleVideo, Inc.

TITLE: PCB SCHEMATIC 912/920 CONT. BD. 565

SIZE D | SHT 2 OF 6 | DRAWING NO. 2009300 | REV L1

DISPLAY RAM ADDRESS

+ RAMA9
A9
A10
A2
A5
A4
A1
A7
A6
A8
+ RAMA8

+ A3
A9
A10
A2
A5
A4
A1
A7
A6
A8
+ A0

A24 LS157
A25 LS157
A26 LS157

A27 LS139

+ PG SEL
-CS3
-CS2
-CS1
-CS0

+5V
R36 4.7K
A21 74LS86

A12 2114-3
A10 2114-3
A6 2114-3
A11 2114-3
A9 2114-3
A7 2114-3
A5 2114-3
OPT

A13 DP8304

+ DB7
+ DB0
+ RD PULSE

+ RD OR WRT
+ A11
A40 LS00
A39 LS32
+ ADV RD OR WRT
- WRT PULSE

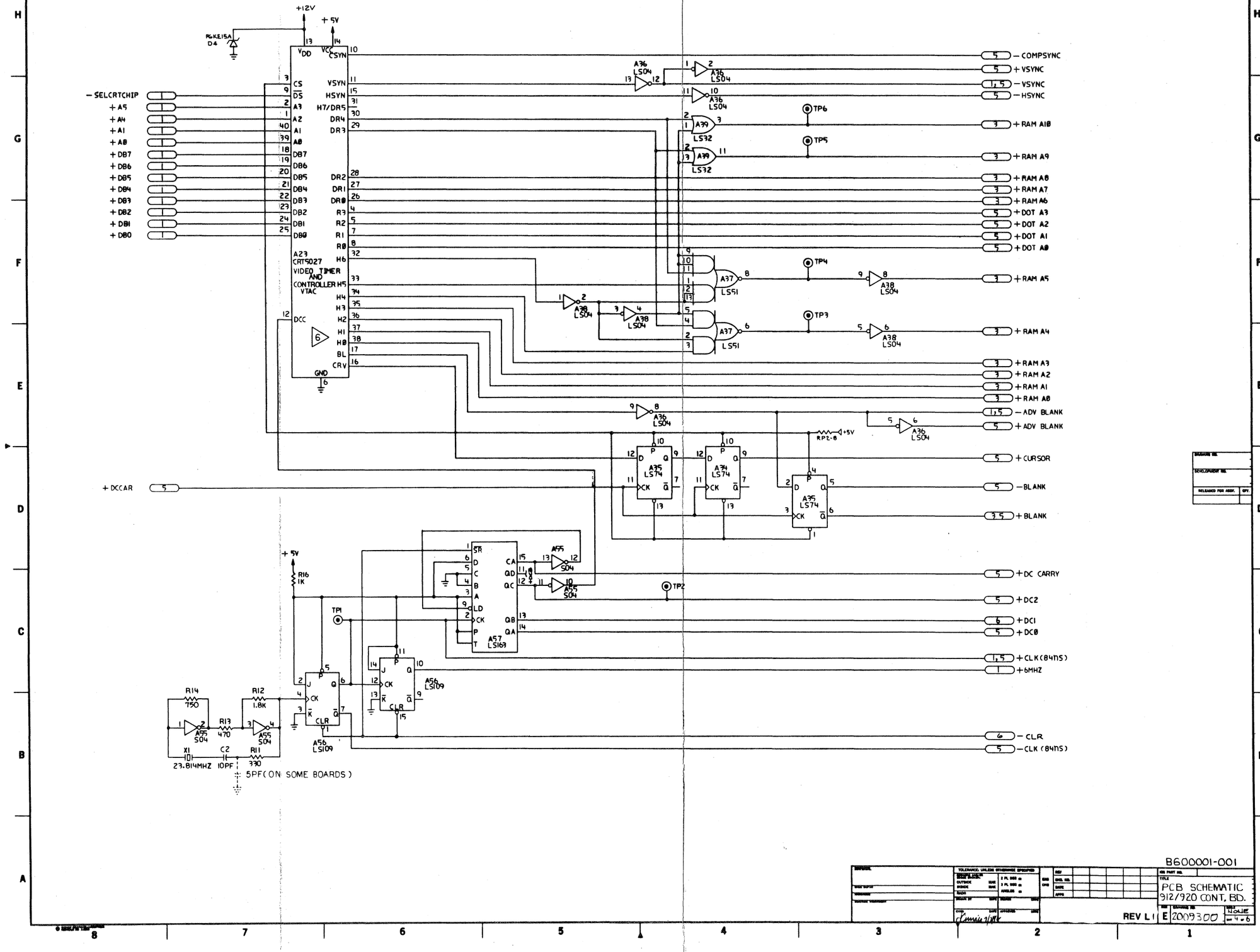
+ DISPDATA 7
+ DISPDATA 0
- CPACC

B600001-001

PCB SCHEMATIC
912/920 CONT. BD.

REV L1

E 2009300



B600001-001

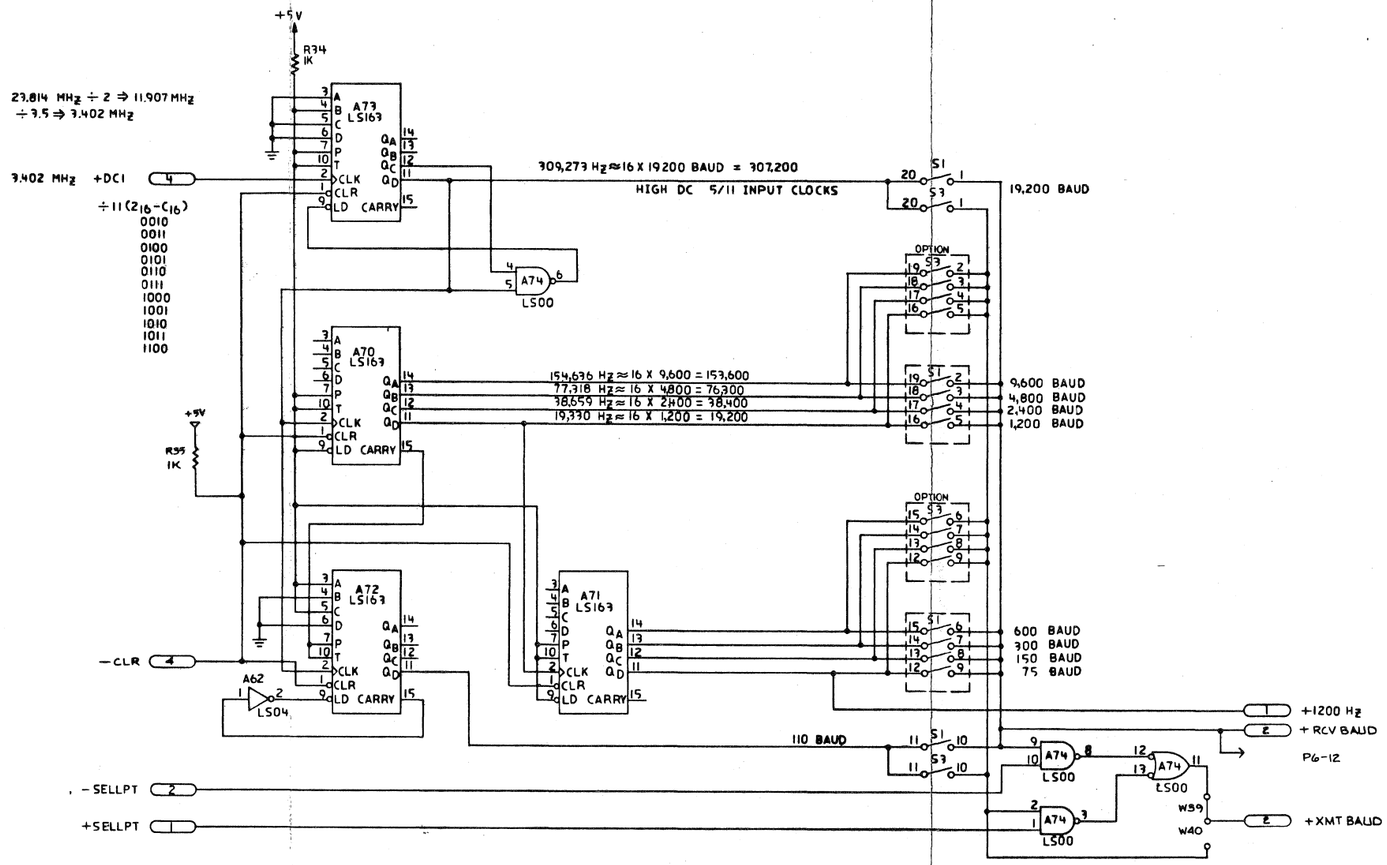
PCB SCHEMATIC 912/920 CONT. BD.

REV L1

E 2009300

SHT 4 of 6

+CURSOR
+4HZ FLASHER
-BLANK
+ADV BLANK
-VSYNC
-10TH DOT ROW
1ST LINE
+DOTA3
+DOTA2
+DOTA1
+DOTA0
+DC0
-ALE
-CPACC
+DC2
+DISP DATA 7
+DISP DATA 0
+DC CARRY
+CLK
-CLK
-ADV BLANK
-CONTROL
+V SYNC
+BLANK
+FORCE BLANK
-COMP SYNC
-H SYNC
CURS FLASH
PROTECT =1/2 INTENSITY
+DCCAR
LOW
"2716" W30
S2
+DRD0
+DRD1
+DRD2
+DRD3
+DRD4
+DRD5
+DRD6
+DRD7
UNDERLINE
INVERT VIDEO
W42
W41
CR
IN914
Q1 2N2219
+VIDEO
VIDEO SHIELD GND (+TTL VIDEO)
+V SYNC
+HSYNC
NE555
VCC RST
THR
DISCH OUT
CTLV
GND
PCB SCHEMATIC
912/920 CONT. BD.
REV L1
B600001-001
E 2009300
SHEET 5 of 6



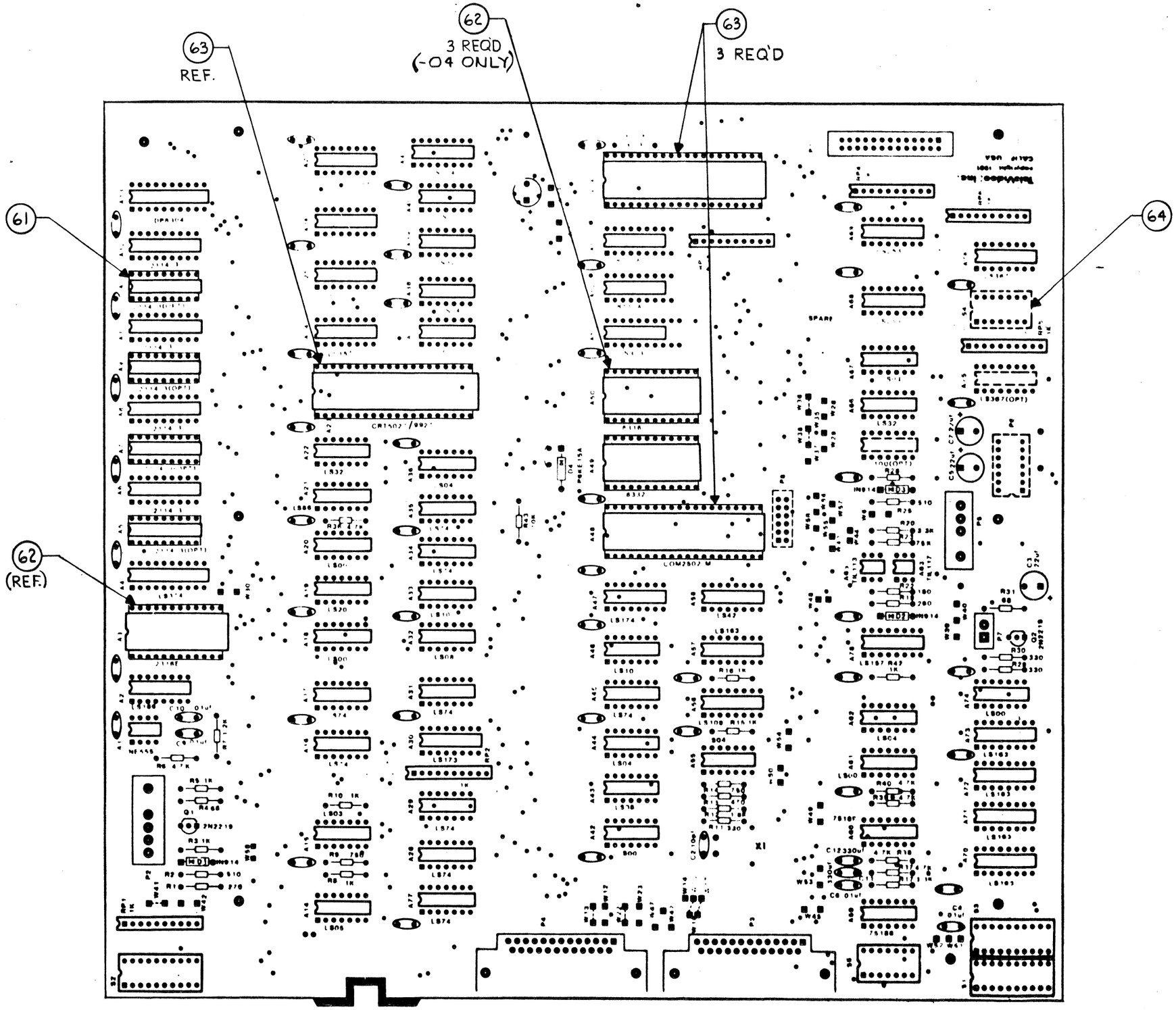
BAUD RATE GENERATION

B60000-001

PCB SCHEMATIC
912/920 CONT. BD.

REV L 1

E 2009300


63
REF.
62
3 REQ'D
(-04 ONLY)
63
3 REQ'D
61
64
62
(REF.)

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	K	L	E	G	H							
1	1	1	1	1	1					C2	Cap DIP Mica 10pf 100D03	2024100
2	3	3	3	3	3					C3,6,7	Cap R/L 22uf 15V	2025700
3	1	1	1	1	1					C1	Cap R/L 1uf 15V	2027901
4	47	47	47	47	47					unmarked	Cap C/D .01uf 20% 16V	2028700
5	1	4	1	1	1					C10	Cap C/D .01uf 10% 50V Y5P	2028900
6	2	2	0	0	2					C11,12	Cap C/D 330pf 50V 20%	2029100
7	1	1	1	1	1					A42	IC 74S00	2024000
8	5	5	5	5	5					A18,20,40,61.74	IC 74LS00	2024200
9	1	1	1	1	1					A15	IC 74LS03	2024400
10	1	1	1	1	1					A55	IC 74S04	2024600
11	5	5	5	5	5					A36,38,44,62,67	IC 74LS04	2024800
12	1	1	1	1	1					A14	IC 74LS05	2025000
13	2	2	2	2	2					A32,43	IC 74LS08	2025200
14	2	2	2	2	2					A33,46	IC 74LS10	2025400
15	1	1	1	1	1					A19	IC 74LS20	2025600
16	3	3	3	3	3					A22,39,66	IC 74LS32	2025800
17	1	1	1	1	1					A58	IC 74LS42	2026000
18	1	1	1	1	1					A37	IC 74LS51	2026200
19	1	1	1	1	1					A17	IC 74S74	2026400
20	8	8	7	8	8					A16,28,29,31,34,	IC 74LS74	2026600
										35,45,77		

NOTES:

TITLE
CONTROL BOARD, TVI-912/920 TERMINAL

DATE
02-01-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	K	L	E	G	H							
21	1	1	1	1	1					A21	IC 74LS86	2026800
22	1	1	1	1	1					A56	IC 74LS109	2027000
23	1	1			1					A27	IC 74LS139	2027200
24	4	4	3	4	4					A24,25,26,78	IC 74LS157	2027400
25	5	5	5	5	5					A57,70-73	IC 74LS163	2027600
26	1	1	1	1	1					A2	IC 74LS166	2027800
27	1	1	1	1	1					A30	IC 74LS173	2028000
28	2	2	2	2	2					A41,47	IC 74LS174	2028200
29	2	2	2	2	2					A68,69	IC 75LS253	2028400
30	1	1	1	1	1					A76	IC 74LS367	2028600
31	1	1	1	1	1					A51	IC 74LS373	2028800
32	1	1	1	1	1					A4	IC 74LS374	2029000
33	1	1	1	1	1					A59	IC 75188N	2029200
34	1	1	1	1	1					A60	IC 75189AN	2029400
35	1	1	0	0	1					A65	IC H11G3	2034200
36	1	1	1	1	1					A63	IC TIL117, 4N37	2029300
37	1	1	1	1	1					A3	IC 2316 ROM A3-2	2034600
38	1	1	1	1	1					A1	IC NE555	2030200
39	1	1	1	1	1					A13	IC DP8304	2030400
40	2	2	2	2	2					A52,53	IC AMD2111-4A	2030600
41	1	1	1	1	1					A48	IC 2502, AY-5-1013A	2030800

NOTES:

TITLE: CONTROL BOARD, TVI-912/920 TERMINAL

DATE: 02-01-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	K	L	E	G	H							
42	1	1	1	1	1					A23	IC 5027,5037,TMS9927	2031000
43	1	1	1	1	1					A54	IC Microprocessor P8035	2031200
44	4	4	4	4	4					A6,8,10,12	IC TMS4045-25NL, 2114 300NS	2035800
45			(4)	(4)	(4)					A5,7,9,11	IC TMS 4045 Option-2nd page	
46			0	1	1					A49B	IC 8332A 32K ROM A49B	2032600
47			0	1	1					A49C	IC 8332A 32K ROM A49C	2032600
48			(1)	0	0					A49R	IC 2316 16K ROM A49R	2032200
49			(1)	0	0					A50R	IC 2316 16K ROM A50R	2032400
50	1	1									IC A49C1	2034000
51	1	1	1	1	1					S5	Dip Switch 7 Pos Top	2174200
52	1	1	(1)	1	1					S3	Dip Switch 10 Pos Top	2181000
53	2	2	2	2	2					S1,2	Dip Switch 10 Pos Side	2096800
54	2	2	(2)	2	2					P3,4	Connector RS232 R/A	2097800
55	4	4	4	4	4					XA5,7,9,11	Socket IC 18 Pin	2098400
56			1	1	1					XA49	Socket IC 24 Pin	2098401
57	3	3	1	1	1					XA50	Socket IC 24 Pin	2098401
58	3	3	2	2	2					XA23,54	Socket IC 40 Pin	2098402
59	1	1	0	0	1					XS4	Socket IC 14 Pin	2098403
60	1	1	1	1	1					X1	Cry 23.814 MHz Fundamental	2098600
61	1	1	1	1	1					P7	Plug 2 Pin	2098501
62	2	2	2	2	2					P2,5	Plug 5 Pin	2098706

NOTES:

TITLE: CONTROL BOARD, TVI-912/920 TERMINAL

DATE: 2-1-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	K	L	E	G	H							
63	1	1	1	1	1					P1	Plug 26 Pin	2098701
64	2	2	2	2	2					R4,31	Res C/F 68 Ohm 5% 1/4W	2051100
65	1	1	1	1	1					R22	Res C/F 180 Ohm 5% 1/4W	2053300
66	2	2	2	2	2					R1,19	Res C/F 270 Ohm 5% 1/4W	2051300
67	3	3	4	4	4					R11,20,29,30	Res C/F 330 Ohm 5% 1/4W	2051500
68	1	1	1	1	1					R13	Res C/F 470 Ohm 5% 1/4W	2051700
69	2	2	3	3	3					R2,14,25	Res C/F 510 Ohm 5% 1/4W	2051900
70	2	2	1	1	1					R9	Res C/F 750 Ohm 5% 1/4W	2031700
71	6	6	6	6	6					R3,5,8,10,15,16	Res C/F 1K Ohm 5% 1/4W	2052100
72			1	0	0					R34	Res C/F 1K Ohm 5% 1/4W	2052100
73	2	2	0	0	2					R41,42	Res C/F 1K Ohm 5% 1/4W	2052100
74	1	1	1	1	1					R7	Res C/F 1.2K Ohm 5% 1/4W	2031900
75	1	1	1	1	1					R12	Res C/F 1.8K Ohm 5% 1/4W	2052300
76			1	1	1					R17	Res C/F 3.3K Ohm 5% 1/4W	2052700
77	2	2	3	3	0					R18,32,33	Res C/F 3.3K Ohm 5% 1/4W	2052700
78	1	1	1	1	1					R6	Res C/F 4.7K Ohm 5% 1/4W	2053100
79	5	5	0	0	5					R36-40	Res C/F 4.7K Ohm 5% 1/4W	2053100
80		1	0	0	1					R23	Res C/F 51K Ohm 5% 1/4W	2032300
81	1									R23		2032500
82			1	1	0					R23	Res C/F 1M Ohm 5% 1/4W	2031500
83	5	5	4	4	4					RP1,2,4,6	Res Pack 1K Ohm	2040500

NOTES:

TITLE: CONTROL BOARD, TVI-912/920 TERMINAL

DATE: 2-1-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	K	L	E	G	H							
84	1	1	0	1	1					RP3	Res Pack 6.2K Ohm	2040700
85		1								R43	Res C/F 10K Ohm 5% 1/4W	2033300
86	2	2	2	2	2					Q1,2	TR 2N4401	2045500
87	3	3	3	3	3					D1,2,3	Diode 1N914	2047500
88		1									P6KE15A Diode	2047900

NOTES:

TITLE CONTROL BOARD, TVI-912/920 TERMINAL

DATE 2-1-83

TeleVideo Systems, Inc.